

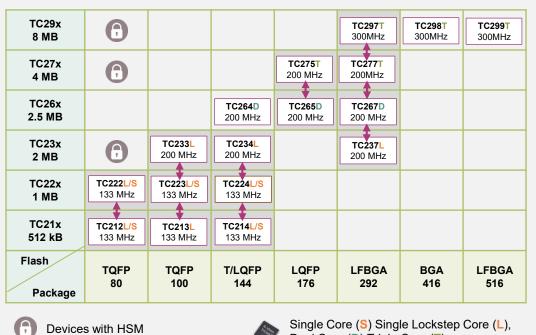
AURIX[™] safety & security introduction and AUTO PSoC[™] ecosystem

Omar Triki 06.10.2021



AURIX™: TC2xx Scalable Family From low cost to high performance applications









Dual Core (D) Triple Core (T)



Upgrade/Downgrade path with pin compatible packages



PRO-SIL™: Safety supporting features

MCU Scalability

- Performance & Flash
- Software and Pin compatibility
- Diverse timer architecture

Power Consumption

On-chip DC/DC high-efficiency power supply

Safety Concept

- PRO-SIL™ ISO26262 / IEC61508 compliance
- > HW redundancy options

Security Concept

Selected devices with Hardware Security Module (HSM)

Availability

All devices are in mass production

Tools & Boards

Multiple options available

AURIX™ TC3xx Architecture Evolution (enhancements vs. AURIX™)



Performance

- New TriCore™ 162 generation
- New instructions
- y up to 6 CPUs @300MHz
- New direct Flash access path

Memories

- Larger SRAM
- > SRAM/Flash ratio increased
- enhanced MPU

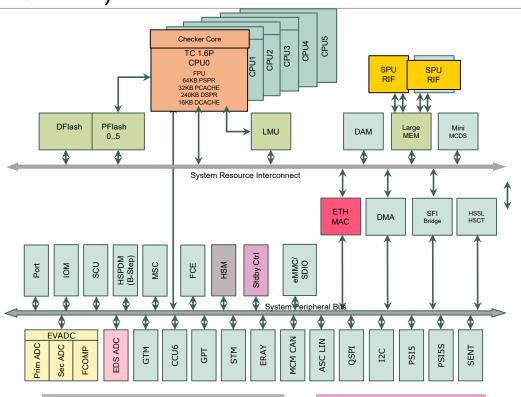
ADC

2021-10-06

- Improvement of existing ADC
- > Reduction of capacitive load

Delta-Sigma:

> enhanced concept



HSM: Full Evita compliance

- > New accelerators ECC256 / SHA256
- Available on all devices

Standby Control Unit

Low power modes

ADAS

New SPU concept

Safety

- LBIST
- MBIST upgrade

Ethernet

-) 1GBit/s ETH
- QoS services

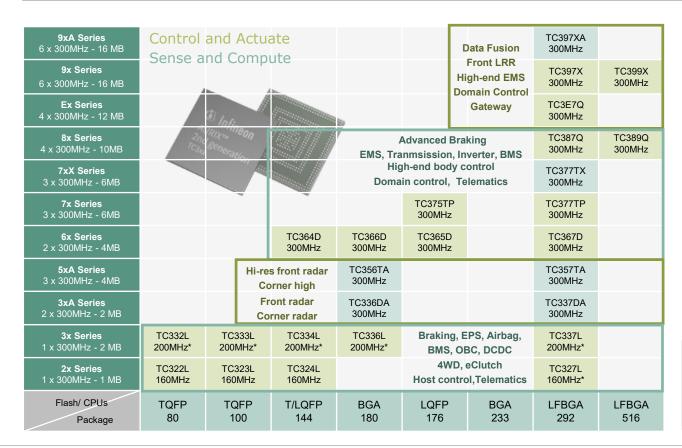
IO Pads

all 5V/3.3V

AURIX™ TC3x – Portfolio

infineon

From low-cost to high-performance applications



MCU Scalability

- > Performance & Flash
- Software compatibility
- Pin-compatibility

Safety/Security Concept

-) ISO26262 ASIL-D compliance of all devices
- > EVITA Full hardware security support on all devices

Connnectivity

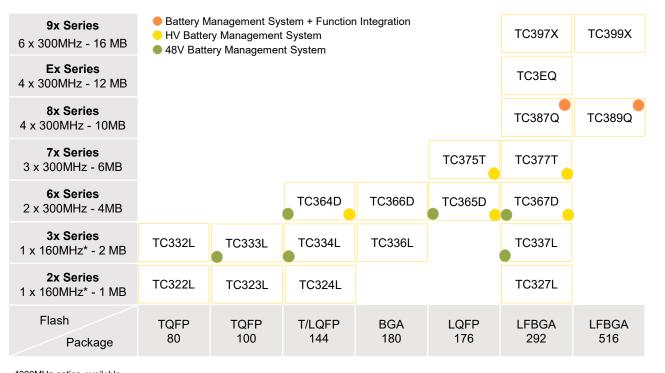
- > Ethernet: up to 2x 1GBit/s
- > CAN FD: up to 16 ch
- LIN: up to 24 ch
-) eMMC IF: for external Flash
- > IPC: up to 2x 320MBit/s
- L Single Lockstep Core
- D Dual Core
- T Triple Core
- Q Quadruple Core
- X Sextuple Core

* 300MHz Option

AURIX™ TC3xx – Portfolio for Powertrain Applications



Devices from low-cost to high-performance suit different BMS requirements



Key AURIX [™] TC3xx feature by application	вмѕ
High Multicore Performance	V
Rich peripheral set	
CAN-FD (up to x2)	V
High RAM content	\checkmark
Timer across family	
Low power modes	\checkmark
Safety (ASIL-D)	V
Security	\checkmark
Resolver-less solution	
SOTA support	\checkmark
High temp. support	
High RAM/flash ratio	\checkmark

^{*300}MHz option available

AURIX™ TC3xx solves challenges at tier1s and OEMs for Battery Management Systems (BMS)



Challenge fields for OEMs /T1s in BMS











AURIX™ TC3xx features Implementation of safety measures in HW (LBIST)

> ISO26262 certified from TÜV, ASIL-D supported by whole family

Integrated HSM -EVITA FULL

Symmetric & asymmetric crypto accelerators

Scalable portfolio & seamless migration between generations and applications

Reuse of multiple concepts (SW, FuSa / security concept) 8-bit standby controller with extremely low current consumption

Battery SoH* checks over long parking periods

Software Over The Air (SOTA) update

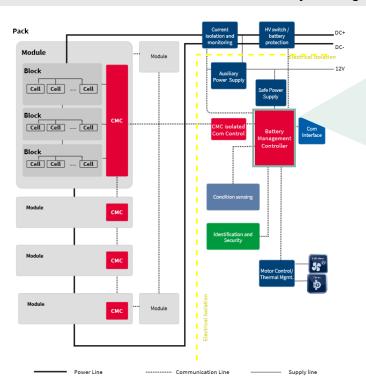
Downtime reduction & SW fallback solution supported

*SoH: State-of-Health

AURIX™ with strong footprint in Battery Management Systems with additional growth expected



MCUs functions for Battery Management Systems (BMS)



- Battery monitoring
 Continous controlling of critical cell characteristics (such as voltage, current, temperature) and calculation of state of charge (SoC) and state of health (SoH)
- Battery protection
 Safety management including crash / mechanical strain detection and Main Switch Control
- Battery lifetime extension
 Optimizing battery life and capacity by e.g. limiting deep battery discharge and actively managing battery temperature

Why AURIX™?

Strong engagement with all relevant market players along the BMS supply chain

- Strong position at EU & Chinese OEMs for 48V and high voltage systems
- Scalable family concept enables re-use across different battery management systems
- Strong product roadmap provides access to innovation
- Proven quality & powertrain knowhow from conventional applications
- Harmonized SW and tool chains between different applications enables SW re-use
- ISO26262 certified from TÜV

AURIX™ Functional Safety concept

Holistic approach with a multitude of hardware measures



HW designed for functional safety

Superior Lockstep CPU with Anti-core in inverse logic

Core



Anti-Core

Holistic safety concept in core, memories, peripherals, buses

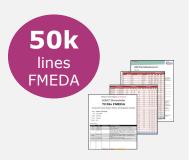
SMU for alarm and fault management in one control point

3-layer access protection:

- Memories
- Peripherals
- Global registers



Everything documented

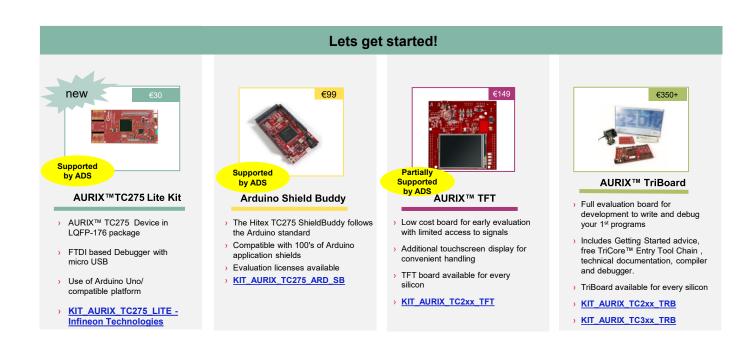


Comprehensive safety manual & Fully Configurable FMEDA

- Provides all relevant information necessary for safety analysis
- Can by tailored to match the user configurations

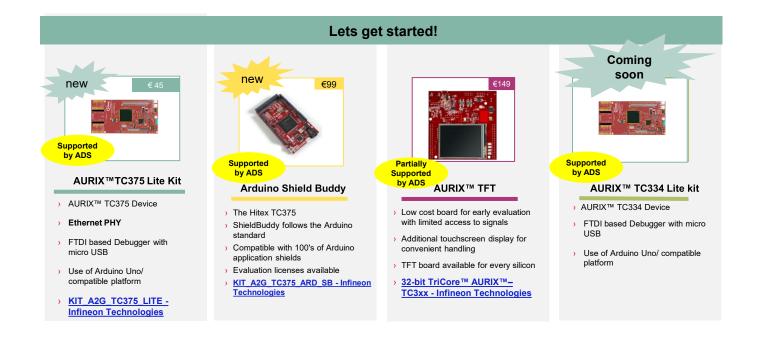
AURIX™ kits – Evaluation and starter Kits





AURIX™ kits – Evaluation and starter Kits









Door handle and foot-kick detection



Optical navigation



Liquid-level sensing



Buttons/sliders



Capacitive navigation



Occupant detection



Touchpads



Biometrics and navigation



Intelligent battery sensors



Touchscreens



Hands-on detection

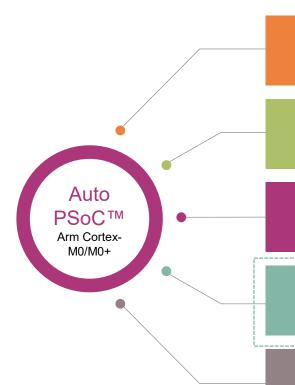


Smart ignition systems



Auto PSoC™ Portfolio





> PSoC 4 S

- Arm M0/M0+ MCU, Programmable Analog, Robust HMI, Scalable platform
- > 16KB 384KB Flash

> PSoC 4 HV MS (Coming Soon)

- > Arm M0+ MCU, Programmable Analog, Robust HMI, 12V LDO, LIN PHY, ASIL-B compliant
- 32KB 512KB Flash

> PSoC 4 HV PA (Coming Soon)

- > Arm M0+ MCU, Precision Analog, 12V LDO, LIN PHY, ASIL-C compliant
- > 64KB 192KB Flash

> PSoC UHV BMS (Coming Soon)

- > Arm M0+ MCU (DCLS), Precision Analog, 110V, BLE, ASIL-D compliant
- > 128KB 256KB Flash

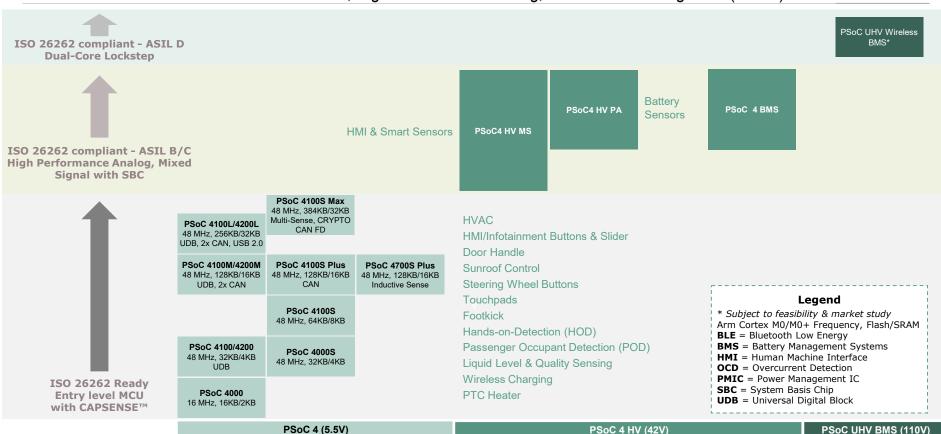
TrueTouch and Fingerprint

- Register-configurable solutions for HMI applications such as touchscreens and fingerprint
- > Very high sensitive capacitive measurements of up to aF (Attofarad)

Scalable PSoC™ 4 Roadmap

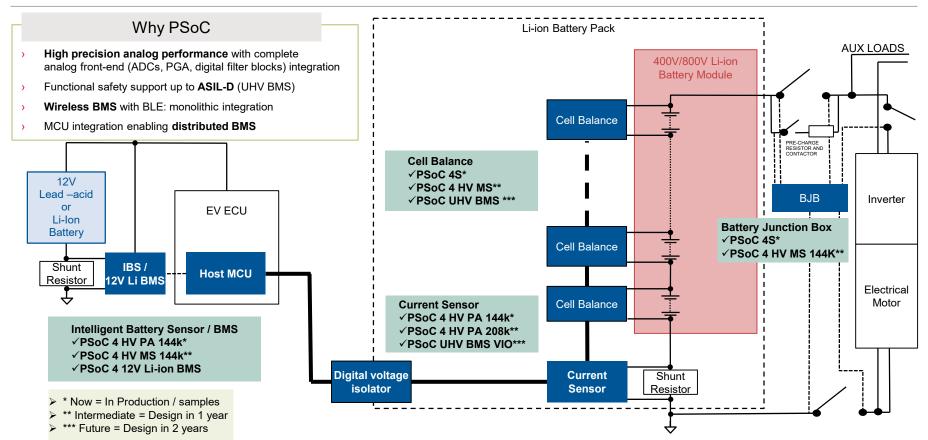


From MCU with CAPSENSE™ to Multi-Sense, High Performance Analog, SBC and BLE integration (Public)



PSoC for BMS







Part of your life. Part of tomorrow.