

1 - DESCRIPTION

This Errata sheet describes the functional and electrical problems known in the C1 revision of the ST10R201-C1 Bondout Chip.

The ST10R201-C1 engineering samples marked as C1-xxxx are not completely tested in all electrical and functional characteristics and should be used for functional evaluation only.

Test conditions for these engineering samples are:

- TA Room Temperature (25°C)
- Vcc 5.0V ±10%
- Fosc 40MHz, PLL disabled, direct drive (f_{CPU} = 40MHz)

2 - FUNCTIONAL PROBLEMS

The following malfunctions are known in this step:

2.1 - PWRDN.1 - Execution of PWRDN Instruction

When instruction PWRDN is executed while pin NMI is at a high level (if PWRDCFG bit is clear in SYSCON register) or while at least one of the port 2 pins used to exit from power-down mode (if PWRDCFG bit is set in SYSCON register) is at the active level, power down mode is not entered, and the PWRDN instruction is ignored.

However, under the conditions described below, the PWRDN instruction is not ignored, and no further instructions are fetched from external memory, i.e. the CPU is in a quasi-idle state.

This problem only occurs in the following situations:

- a) The instructions following the PWRDN instruction are located in an external memory, and a **multiplexed bus** configuration **with memory tristate waitstate** (bit MT-TCx = 0) is used.
Or
- b) The instruction preceding the PWRDN instruction **writes** to external memory or an XPeripheral (XRAM,CAN), and the instructions following the PWRDN instruction are located in external memory. In this case, the problem occurs for any bus configuration.

Note: The on-chip peripherals are still working correctly, in particular the Watchdog Timer, if not disabled, resets the device upon an overflow. Interrupts and PEC transfers, however, cannot be processed. In case NMI is asserted low while the device is in this quasi-idle state, power-down mode is entered.

No problem occurs if the NMI pin is low (if PWRDCFG = 0) or if all P2 pins used to exit from power-down mode are at inactive level (if PWRDCFG = 1): the chip normally enters powerdown mode.

Workaround:

Ensure that no instruction that writes to external memory or an XPeripheral precedes the PWRDN instruction, otherwise insert a NOP instruction in front of PWRDN. When a multiplexed bus with memory tristate wait state is used, the PWRDN instruction must be executed from internal RAM or XRAM.

2.2 - ADAPT: Possible entry in adapt mode

If synchronous power-on reset is used, ST10R201 may enter adapt mode.

Workaround:

Use asynchronous power-on reset (Vpp low for power-on reset).

Note: This behaviour is identical to the one of ST10 products.

2.3 - MAC.1: Pipeline conflict after CoStore operation

After a CoStore instruction with any SFR/ESFR for destination, this SFR/ESFR can not be immediately read in the following instruction due to a pipeline conflict.

Workaround:

To make sure that the new SFR/ESFR value delivered by CoStore is used, at least one instruction must be inserted between CoStore and a subsequent SFR/ESFR-using instruction, as shown in the following example:

```
In      CoStore [R1], MAH ; R1 points to T3 register
In+1    ...                ; must not be an instruction using T3
In+2    ADD T3, #4         ; now, T3 value is correct and can be used.
```

2.4 - ST.BUS.4: Incorrect bus arbitration

The problem arises when the BUS ARBITRATION resource are used.

Correct operation description:

When the chip is in HOLD mode (buses released), to request control of the bus, the chip must assert to one the pin BREQ (P6.7).

Incorrect operation observed:

When the chip is in HOLD mode, the pin BREQ toggles even if the chip needn't to get control of the bus. The problem happens when the program executed is a loop, and all the instructions of the loop are read from the jump cache registers.

In multiplexed mode the problem appears:

- With a two instructions loop (and both instructions are read from the cache jump register).
- With a one instruction loop. If a PEC instruction is injected, a useless bus request is enabled (BREQ = 1).

In demultiplexed mode the problem appears:

- With a one or two instructions loop read from the cache jump register.

Example

```
      bset   HLDEN
LOOP:  jmp   LOOP ; single word cache jump

      nop
LOOP:  jmp   LOOP ; double word cache jump
```

Workaround:

Size of loops should be greater or equal than 4 words (e.g. two double word instructions).

2.5 - Visible.1: Visible mode not correct

When visible mode is enabled (SYSCON.1=1), the accesses to Xperiperahls (read or Write) are made visible to all pins of Port0, whatever the bus configuration.

If all external peripherals are configured in 8-bit mode, an XBUS-peripheral write can cause a conflict on POH.

Workaround:

Visible mode should not be used when 8-bit external bus configuration is selected: 16-bit data transfer on Xbus would require 2 cycles on 8-bit databus, thus impacting real time.

Note: Visible mode cannot cause any conflict on POH with other ST10 products; still only part of the data will be visible (only D0/D7).

2.6 - ST.CPU3: Incorrect addressing with MOV [Rn (+)], [Rm(+)] and PEC transfers

For specific combinations of the value of Rn register (destination address) and the value of Rm register (source address), the effective address of the destination operand will be erroneous.

Affected instruction:

- All MOV instructions (byte or word), like MOV [Rn(+)], [Rm(+)]
- All CoXXX [IDXi(+)], [Rm(+)] like COMAC [IDX0+], [Rm+], except COMOV instruction

This can only happen if:

- CP is within [F200h ...F7FFh]
- IDX_i points within [F200h...F7FFh]

Workaround:

Map register banks (i.e. CP register) in [F800h...FDFh] and IDX_i registers must point within [F800h...FDFh].

2.7 - ST.CPU4: Incorrect addressing with Rn, [Rm(+)] addressing mode

For specific combinations of the value of the address of Rn register and the value of Rm register (source address), the effective address of the destination operand will be erroneous.

Affected instructions:

- All arithmetic instructions (byte or word) like ADD Rn,[Rm(+)]
- All logical instructions (byte or word) like AND Rn, [Rm(+)]
- Compare instructions (byte or word) like CMP Rn, [Rm(+)]
- All DSP instructions with register indirect addressing except CoMOV instruction
Coxxx..., [Rm(+)]
Coxxx..., [Rm(±)QRx]

This can only happen if CP and IDX registers are within [F200h...F7FFh].

Workaround:

Map register banks (i.e. CP register) in [F800h...FDFh] and IDX_i registers must point within [F800h...FDFh].

Note: The low part of the DPRAM, [F200h...F7FFh], can be used for the system stack.

History of fixed functional problems of the ST10R201-C1

Name of the Modification	Short Description	Fixed in Step
CPU.17	Arithmetic Overflow By Divlu Instruction	C1
BUS18	Incorrect Instruction Fetch On Cache Jump	C1
ST.BUS.1	Incorrect Pec Source Fetch After Jmps Instruction	C1
CAPCOM.1	Software Reload Of The Capcom Timer	C1
ADC.11	First Adc Prog. In Autoscan Conversion Mode	C1
ST.ADC.1	Channel Inj Coincident With End Of Scan Conversion	C1
ST.ADC.2	Reset And Set Adst When A Conversion Is In Progress	C1
ST.ADC.3	First Adc Prog. In Autoscan Conversion Mode	C1

3 - DEVIATIONS FROM DC/AC PRELIMINARY SPECIFICATION

DC parameters

Engineering data are not completely collected yet.

AC timings

Engineering data are not completely collected yet.

Note on on-chip oscillator

The XTAL2 output is not designed to provide a valid signal when XTAL1 is supplied by an external clock signal. It may happen, if the external clock signal is not perfectly symmetrical and centered on $V_{DD} / 2$, that XTAL2 signal is not equal to XTAL1. This is due to the design of the oscillator, which has a auto-adaptation gain control dedicated to external crystal.

If an external clock signal is directly provided on XTAL1 pin, then leave XTAL2 pin disconnected to achieve the lowest consumption of the on-chip oscillator.

4 - ERRATA SHEET VERSION INFORMATION

This document was released on the 21th of December 2001. It reflects the current silicon status of the ST10R201-C1.

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