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# Model-Based Design and Virtual ECUs targeting the PPU

## Verification of Heterogenous Multicore Code Generation for Infineon AURIX TC4x Architecture

Stefan Thiel, Synopsys

Sept-24, 2025

# Agenda

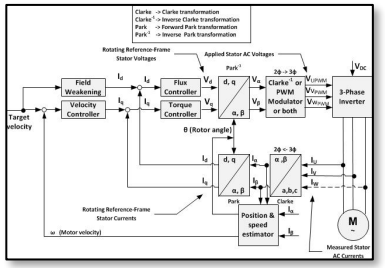
- Case Study
- Model Based Design Flows
- Virtual Hardware Models in the Loop
- Demonstration
- Summary

# Case Study

## Electric Vehicle Control Application

## Target Hardware – AURIX™ TC4x

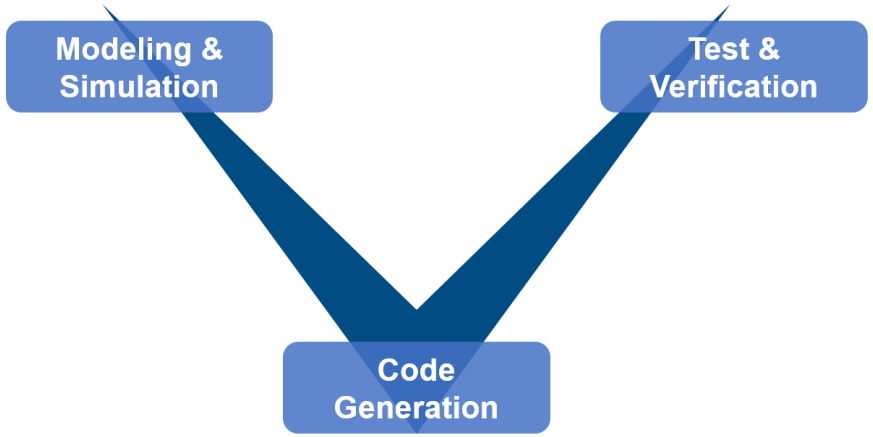
## Virtual Prototype

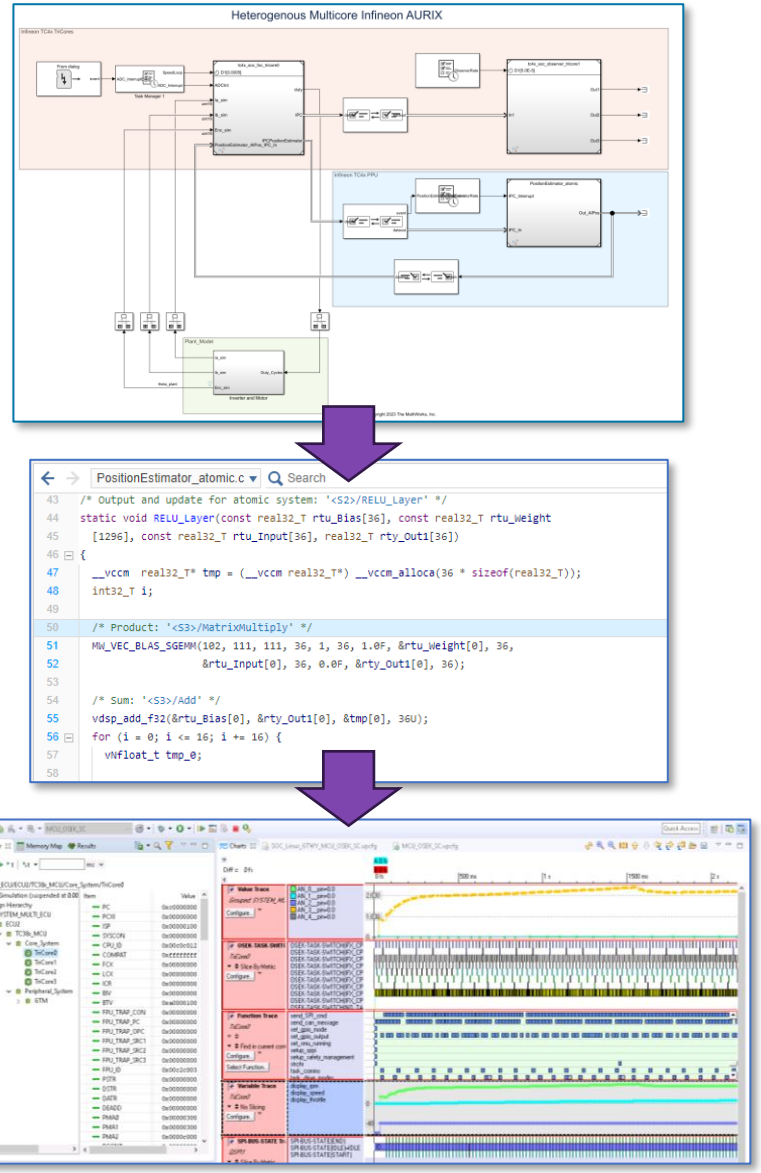



# Case Study: Electric Vehicle Control Application

## What will be covered?

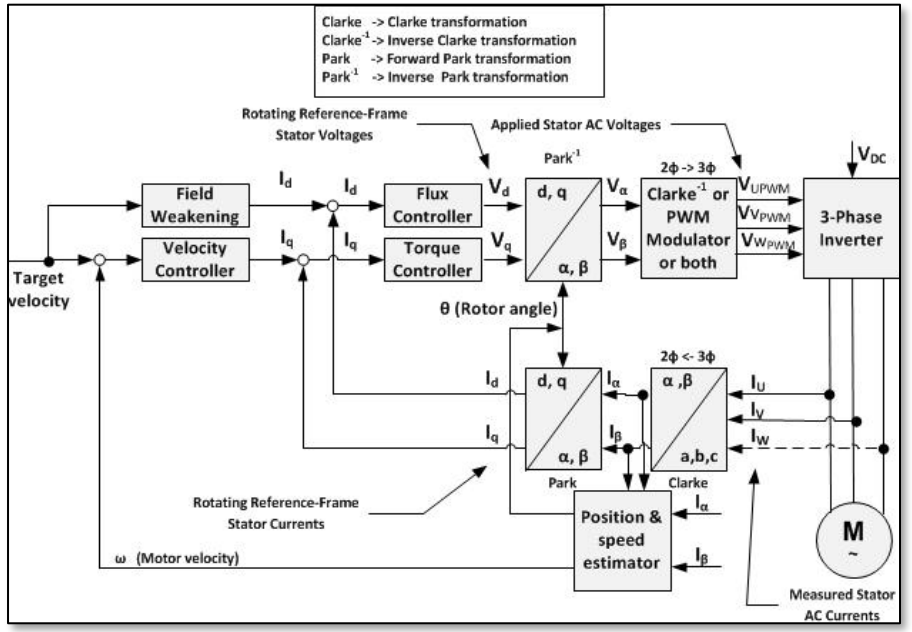
- Modeling and Simulation of FOC-based Motor control
  - Advanced sensor-less algorithms
- Code generation and deployment to AURIX™ TC4x
  - multiple TriCores
  - Optimized code generation and deployment to PPU
- Testing on Virtual-HW-in-the-Loop setup



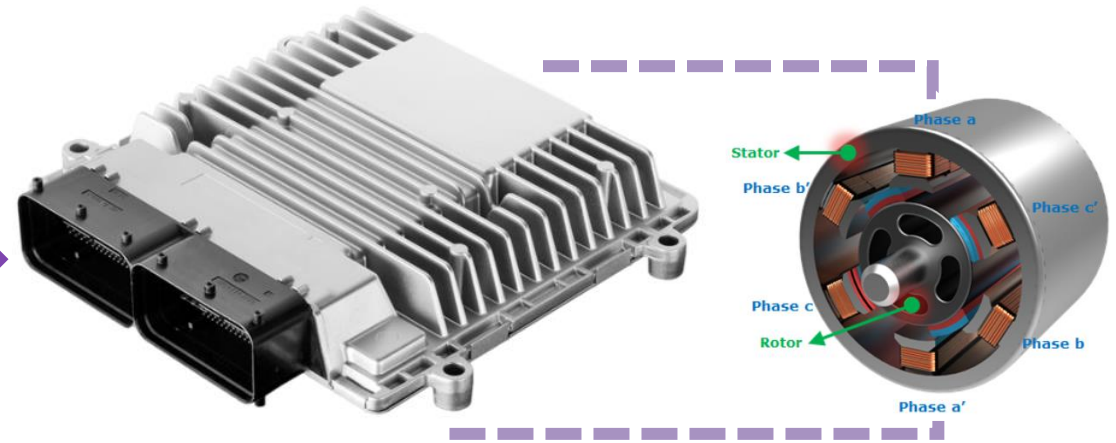



# Case Study: Motor Control Embedded Software Solutions

## Deploying AI Techniques to reduce cost (Sensor-less Field Oriented Control)




Control Algorithm (FOC)




- Use of sensor-less algorithms eliminates the need for speed or position sensor. (cost saving)
- AI techniques such as Multi Layer Perceptron (MLP) can be used to predict speed and position.
- Software can be partitioned into heterogenous hardware according to the processing function required.

# Case Study: Target Hardware

## AURIX™ TC4x

Performance ASIL-D
**Enhanced TriCore™**
With up to 6CPUs @
**500MHz**

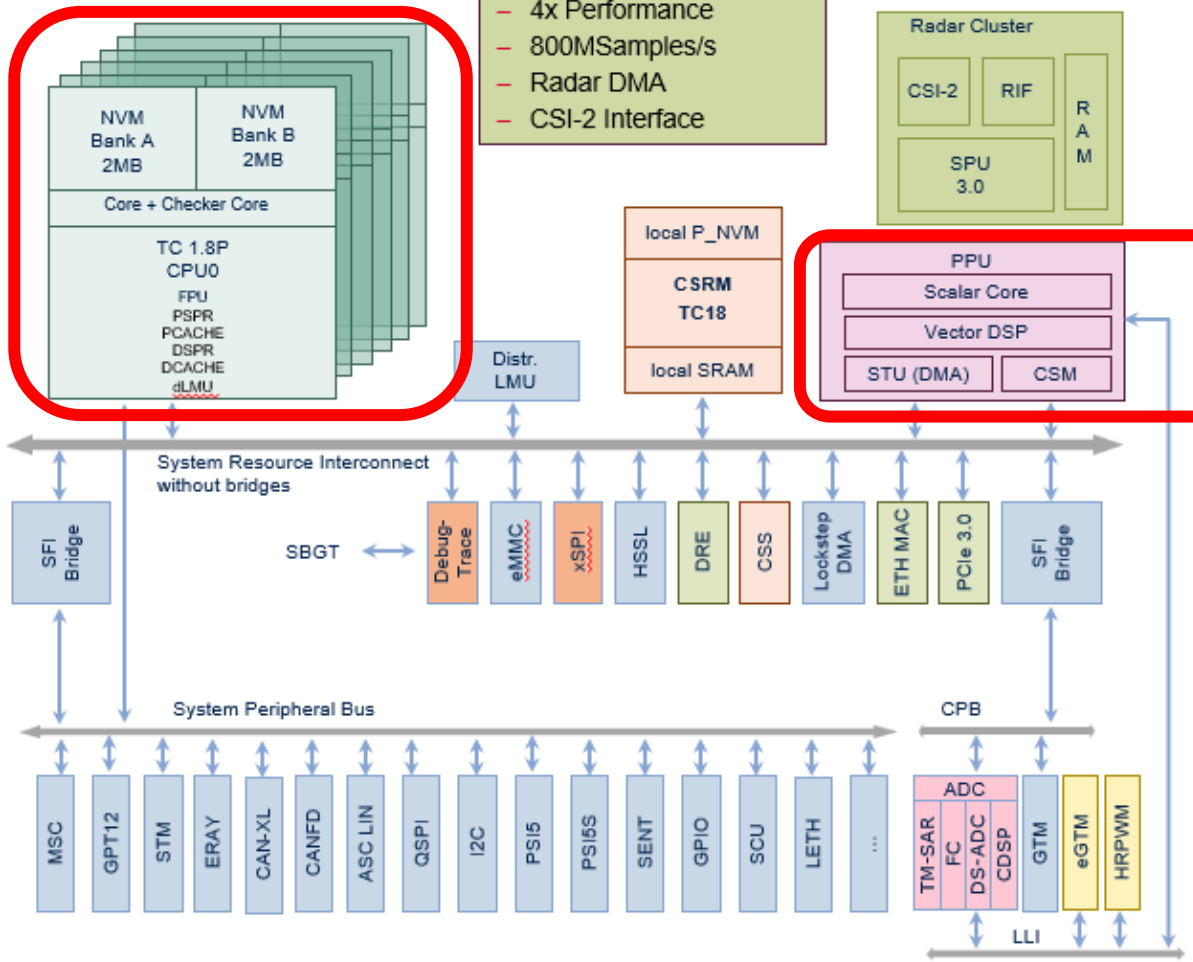
**Bigger Tightly Coupled SRAM** for increased performance

**Full AB-Swap Support**

**Debug and Trace**
Safe and the secure in field

**xSPI**
External Memory Interface

**ADC**
Dedicated DSPs
Enhanced ADCs




**Radar Cluster**
- 4x Performance
- 800MSamples/s
- Radar DMA
- CSI-2 Interface

**CSRM**
New high performance Security Modules with QM support

**CSS**
Dedicated communication security satellites

**New Programmable HW Accelerator - PPU**
**SIMD Vector DSP + Scalar Core** for Modelling and Precise Control – **ASIL D**

**New high-speed comm Interfaces:**
- PCIe 3.0
- 100Mb- 5 Gbps Ethernet

**New 10 Mbit Ethernet and CAN-XL**

**New communication routing accelerator:**
- DRE- Data Routing Engine

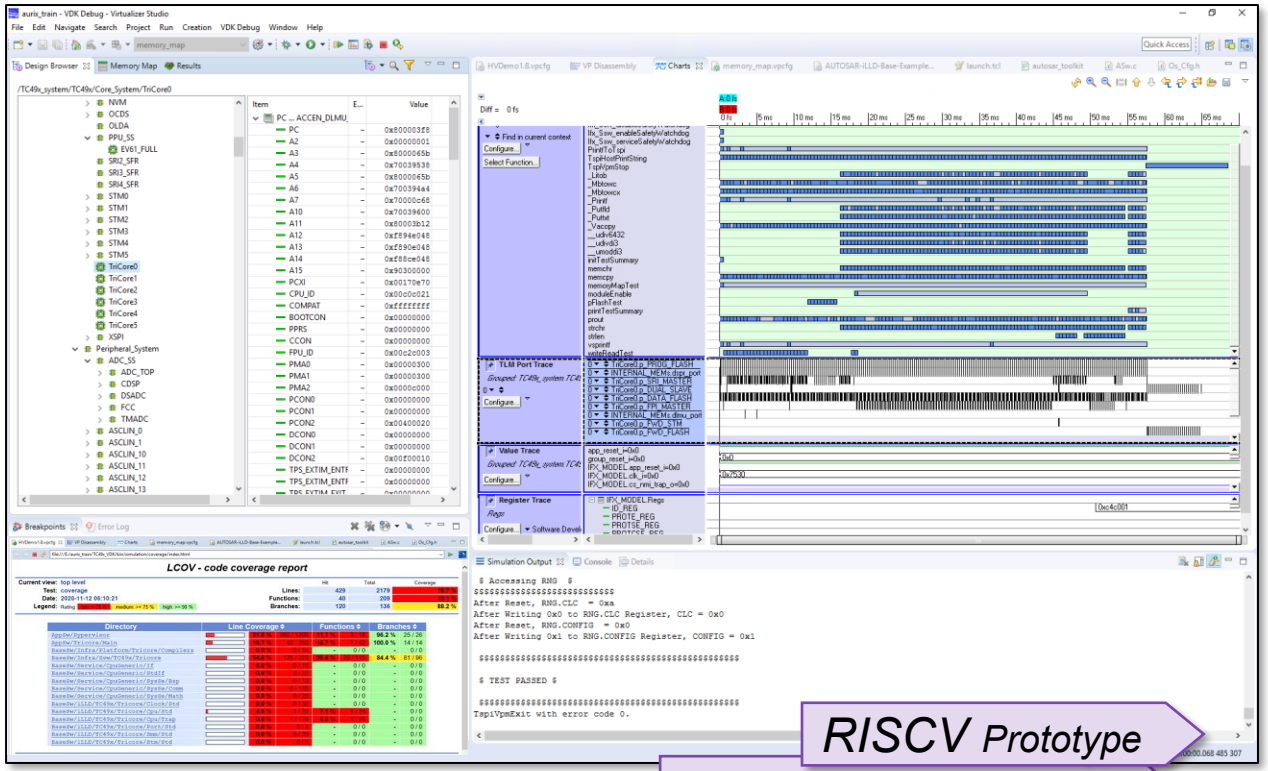
**New eGTM** timers and **High Resolution PWM** with **low latency interconnect (LLI)**

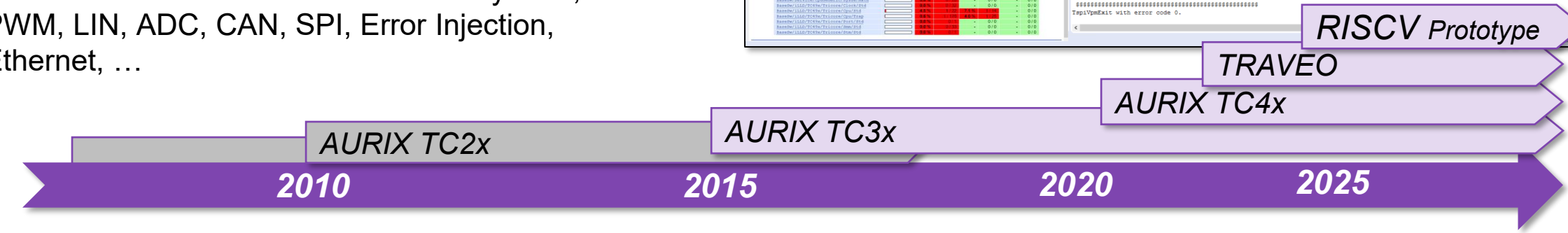
# Collaboration to develop the AURIX TC4xx VDK

Comprehensive core and model coverage for software use cases

## Virtual Prototype High Level Content

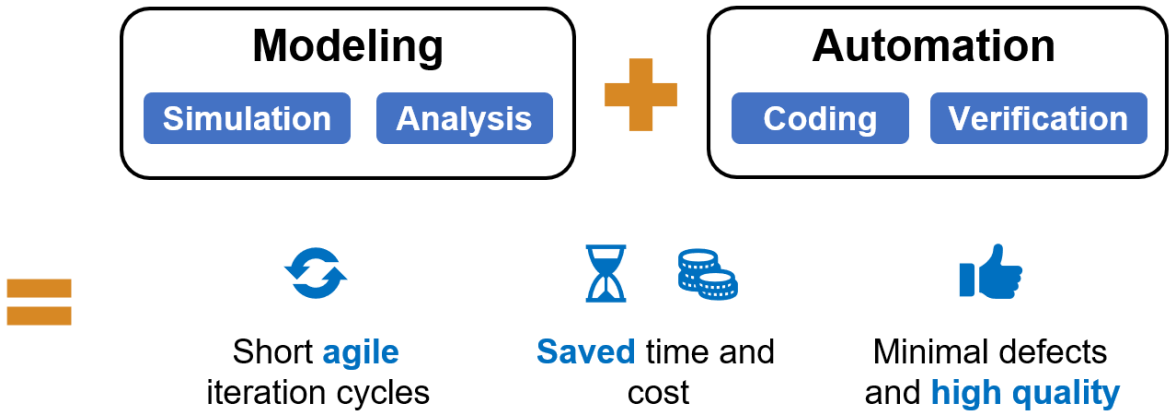
- System: TriCore™ CPU subsystem and PPU
- Memories
- Communication: including SENT, CAN, Ethernet, FlexRay, LIN, …
- Analog-to-digital converters
- Timers including GTM
- Security and Safety
- APIs to external connection for Memory R/W, PWM, LIN, ADC, CAN, SPI, Error Injection, Ethernet, …





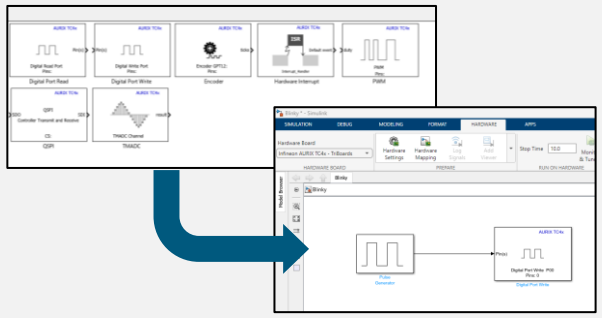
# Model Based Design flows.

Systematic use of models throughout the development process

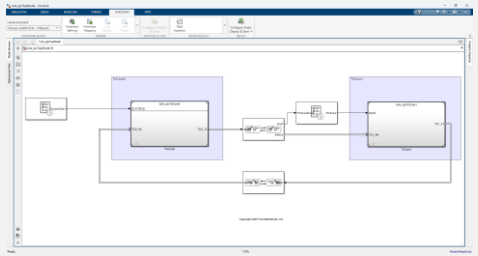


# Model Based Design Code Generation

## The MathWorks TC4x Hardware Support Packages and Heterogenous Flows



Peripheral driver blocks enable hardware peripheral use in deployed Simulink models



Multi-core model example simulates IPC and then deploys to hardware

MathWorks

Embedded Coder Support Package

+

SoC Blockset Support Package


Heterogenous MCU

MATLAB/Simulink Infineon AURIX TC4x Hardware Support

Embedded Coder

Vanilla ANSI 'C'

Code Replacement

ANSI 'C' to ARC DSPLIB function bindings

ARC-optimized 'C'

Synopsys ARC MetaWare Dev Toolkit

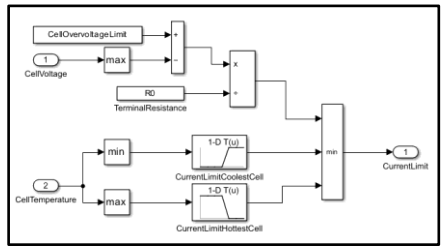
Executable code optimized for running on EV71 (PPU)

MathWorks

Synopsys

Optimized Code Generation flow for PPU

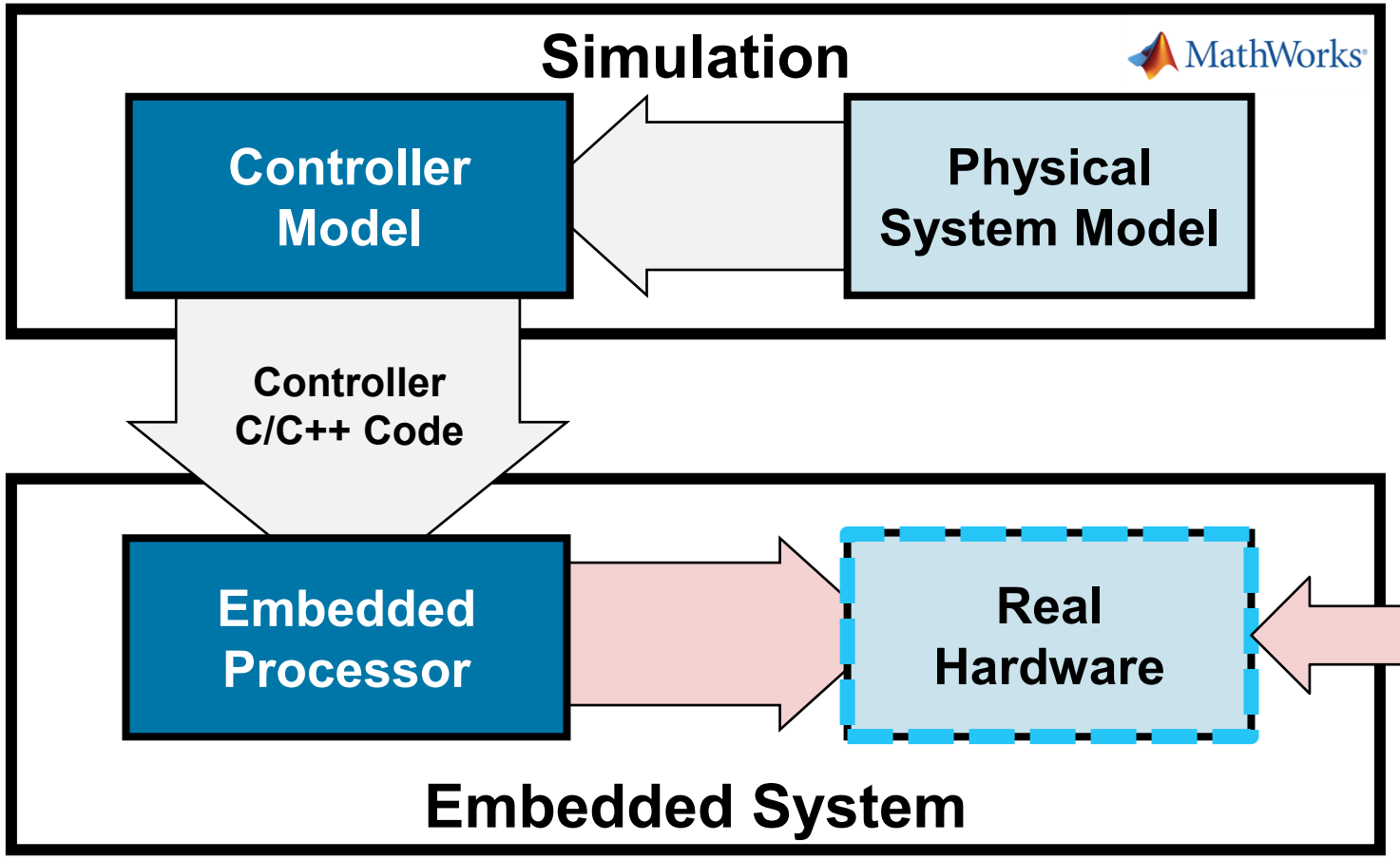
# Embedded software development using code generation

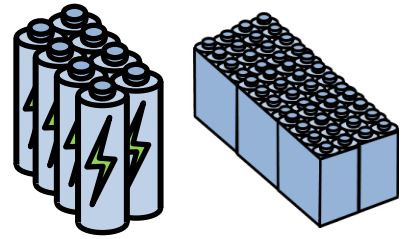



**Control Design & Desktop Simulation**

```
int32_T idx;
__m128 tmp;
__m128 tmp_0;
for (idx = 0; idx <= 136; idx += 4) {
  tmp = _mm_load_ps(&simd_model_U.In1[idx]);
  tmp_0 = _mm_load_ps(&simd_model_U.In2[idx]);
  tmp = _mm_add_ps(tmp, tmp_0);
  tmp_0 = _mm_load_ps(&simd_model_U.In3[idx]);
  tmp_0 = _mm_add_ps(tmp, tmp_0);
  tmp = _mm_load_ps(&simd_model_U.In4[idx]);
  tmp = _mm_add_ps(tmp_0, tmp);
  _mm_store_ps(&simd_model_Y.Out1[idx], tmp);
}
```

**Code Generation**

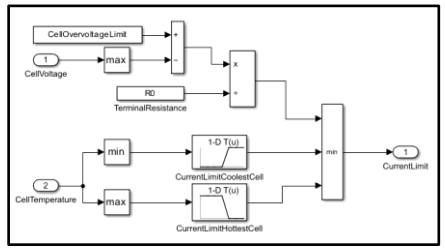


**Physical System**

**Real-Time HIL Testing**

# Virtual Prototype - Removing Hardware Dependencies

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  tmp_0 = _mm_add_ps(tmp, tmp_0);
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  tmp = _mm_add_ps(tmp_0, tmp);
  _mm_store_ps(&simd_model_Y.Out1[idx], tmp);
}
```

**Code Generation**

**Simulation**

MathWorks

**Controller Model**

**Physical System Model**

**Controller C/C++ Code**

**Virtual Prototype (vECU)**

**Embedded System**

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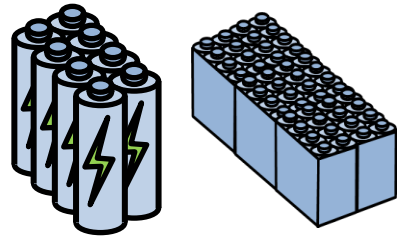
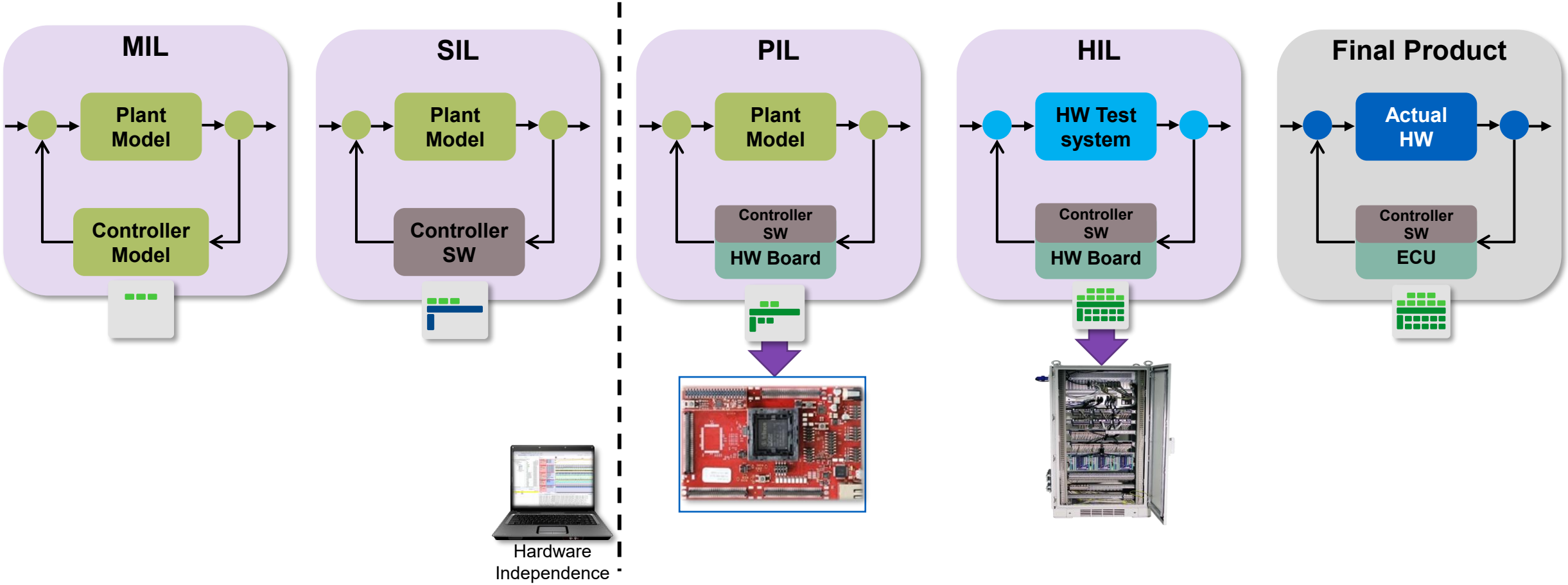


**Physical System**

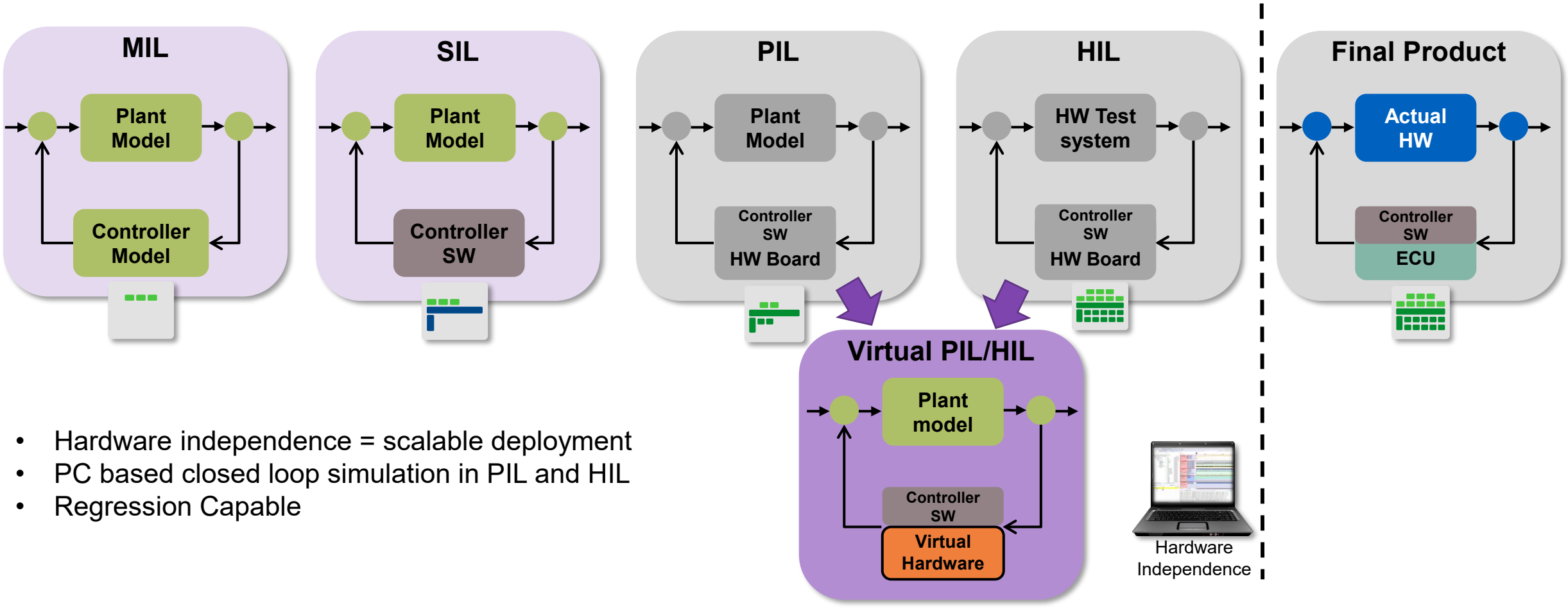
~~Emulation Hardware~~

~~Real-Time HIL Testing~~

# Model-Based-Design Flow with real Hardware

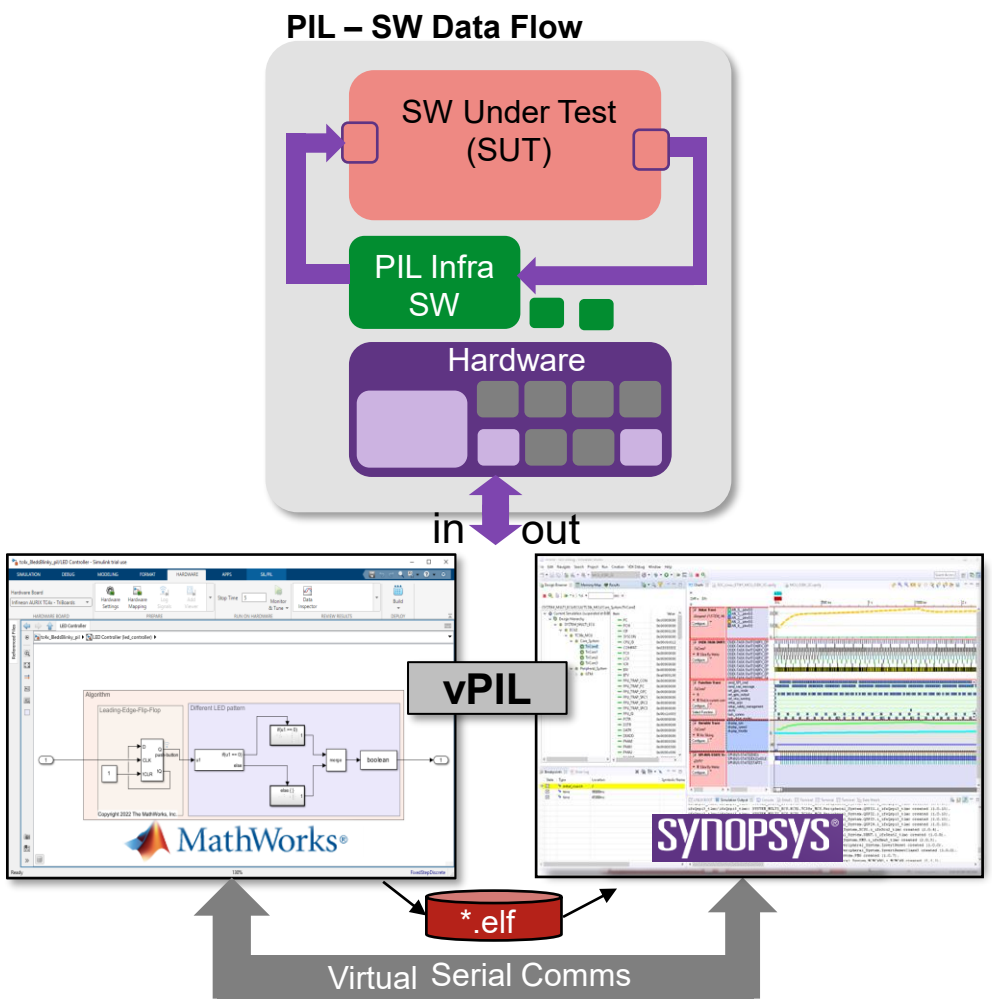


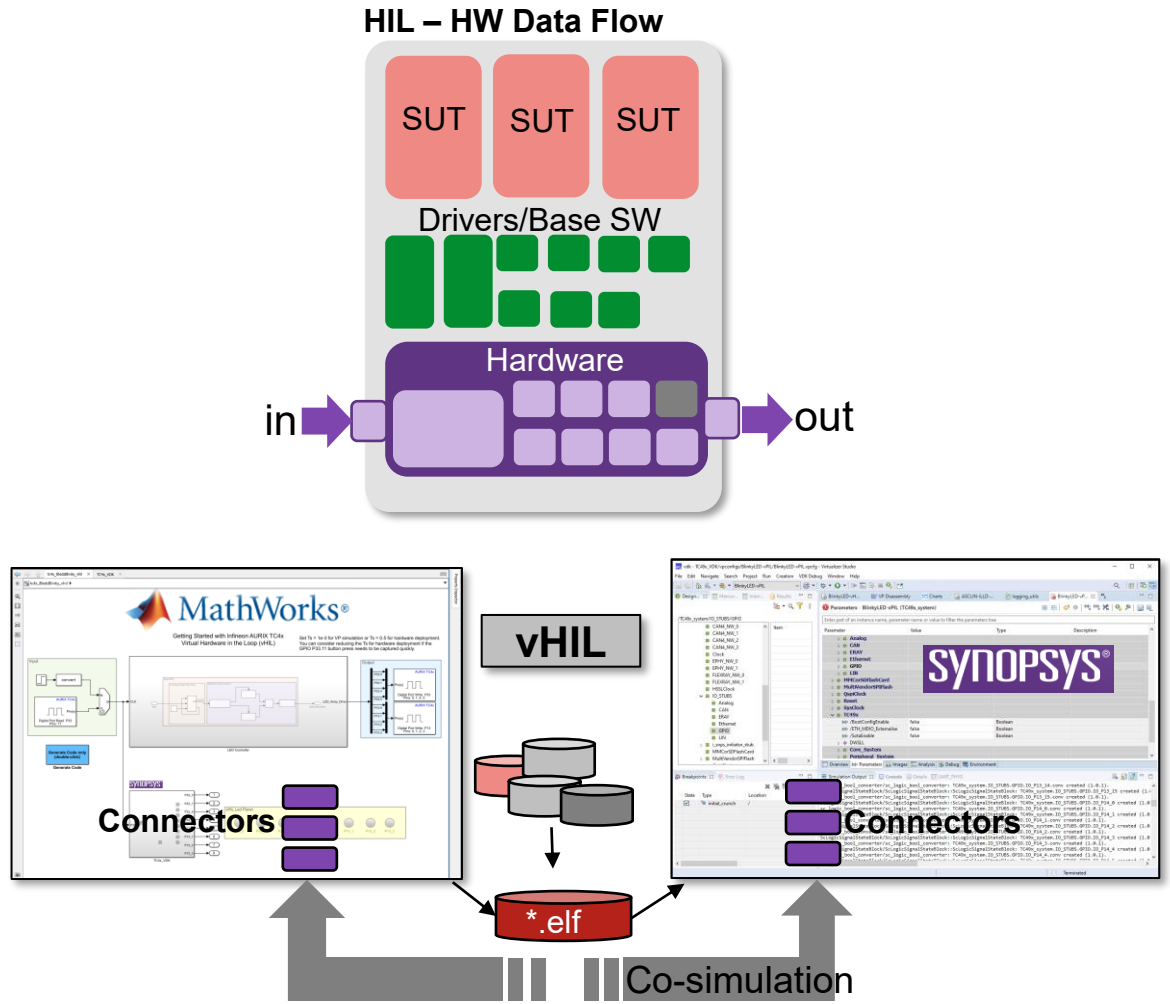
# Model-Based-Design Flow with Virtual Hardware




- Hardware independence = scalable deployment
- PC based closed loop simulation in PIL and HIL
- Regression Capable

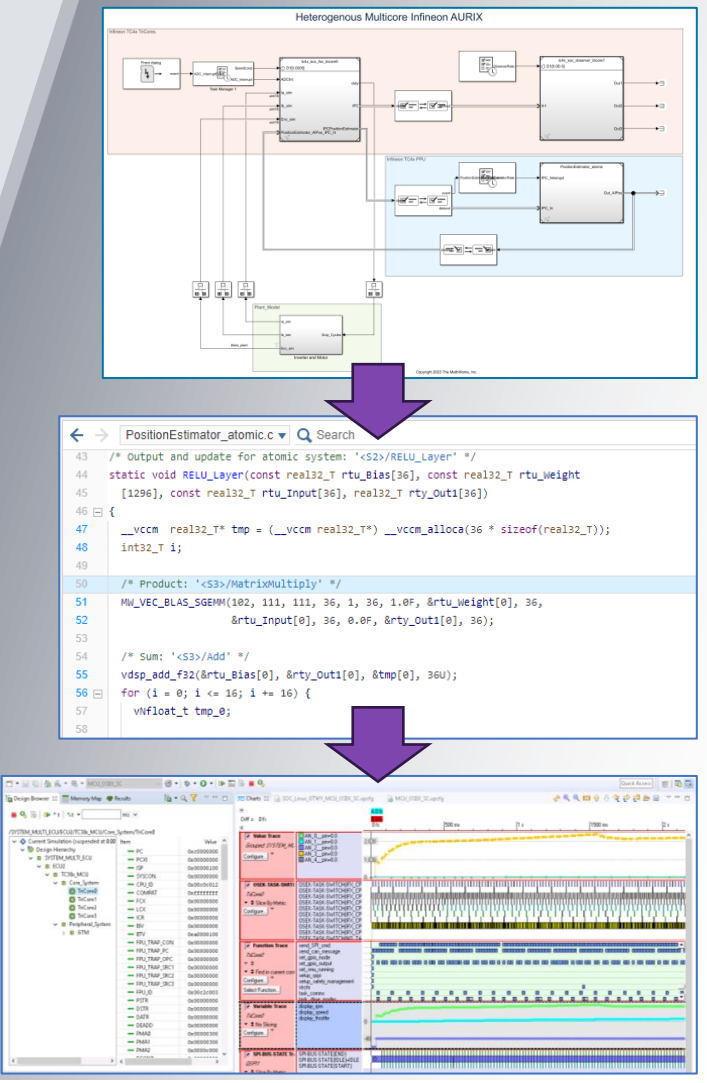
# A Closer Look at Virtual PIL and Virtual HIL



# Summary

- Developing Advanced Sensor-less Motor Control Algorithm
  - Code generation for TC4x HW
- MDB Design Flow & optimized implementation for TC4x
  - Deployment to One or Multiple TriCore
  - Optimized code deployment to PPU
- Synopsys VDK for AURIX™ TC4x
  - Capabilities beyond HW
- Testing on Virtual-HW-in-the-Loop setup
  - Hardware independent efficiency



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# Thank you