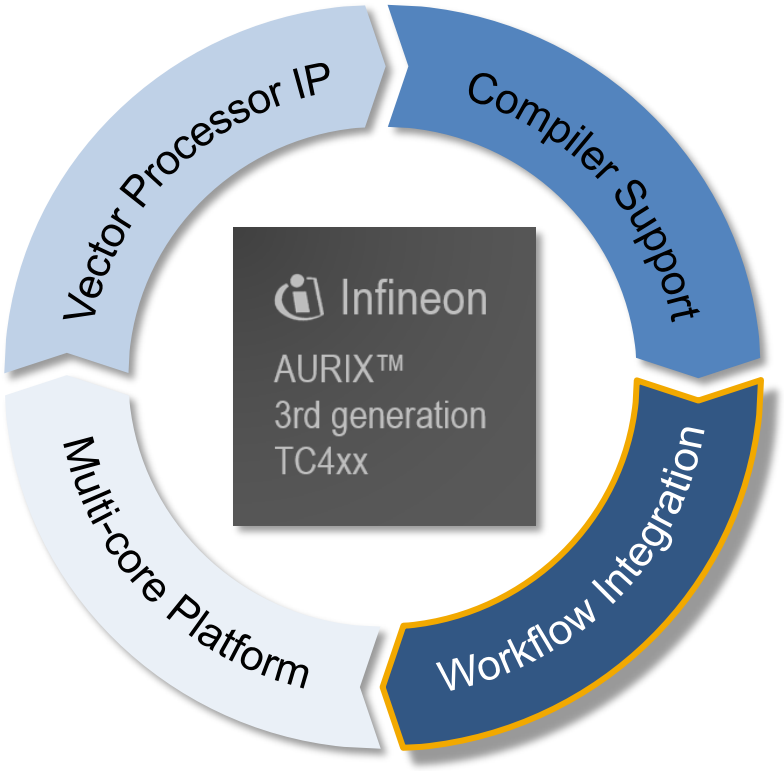
Model-Based Embedded Software Development using MathWorks Hardware Support Package

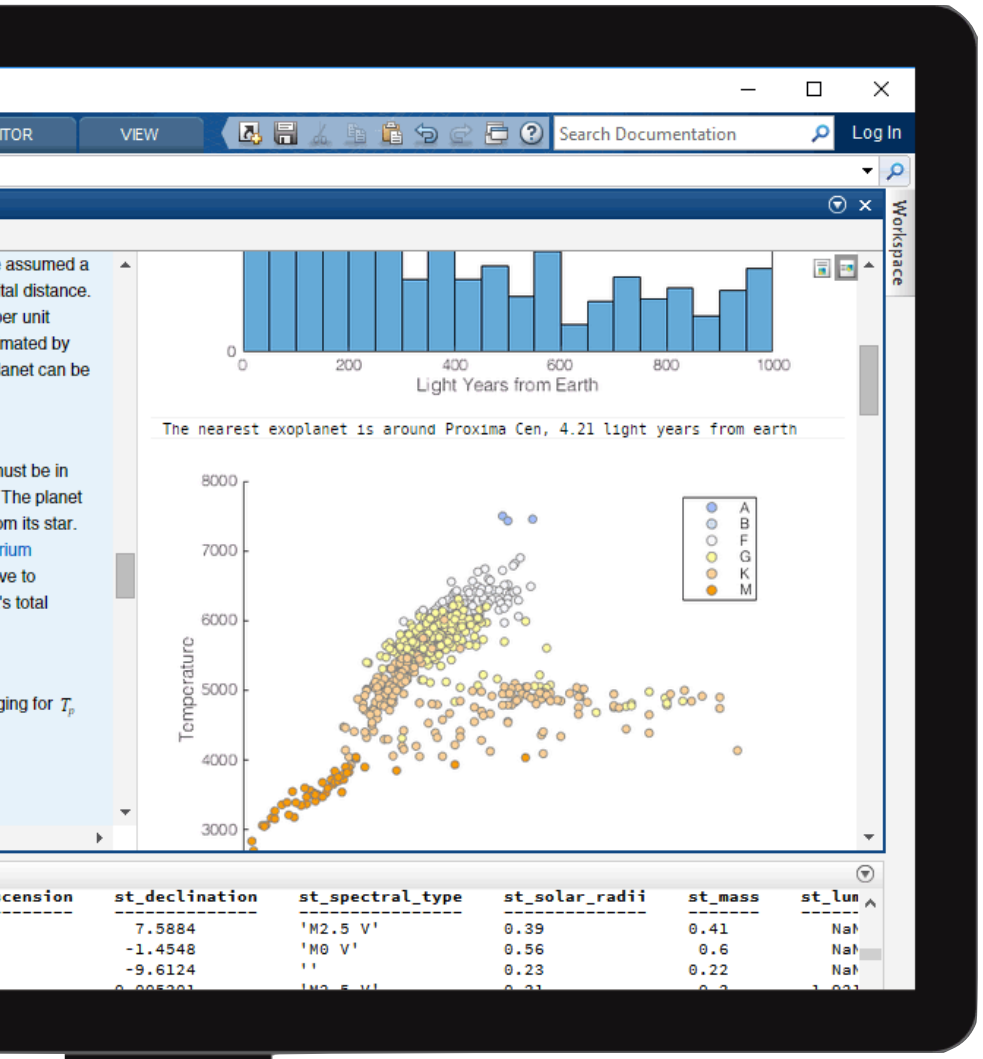


Jayakarthigeyan Prabakar
Product Marketing Manager, MathWorks
jprabaka@mathworks.com

Agenda

- MathWorks Products and Model-Based Design
- Automatic code generation for Infineon AURIX TC3x and TC4x
- Monitor and Tune Workflow
- Multi-Core Modeling with Tricore and PPU
- Summary
- Q&A

MATLAB



Data Analysis

Signal Processing

Predictive Maintenance

Machine Learning

Algorithm Development

Algorithm Development

Mathematical Modeling

Test and Measurement

Simulink and Embedded Coder

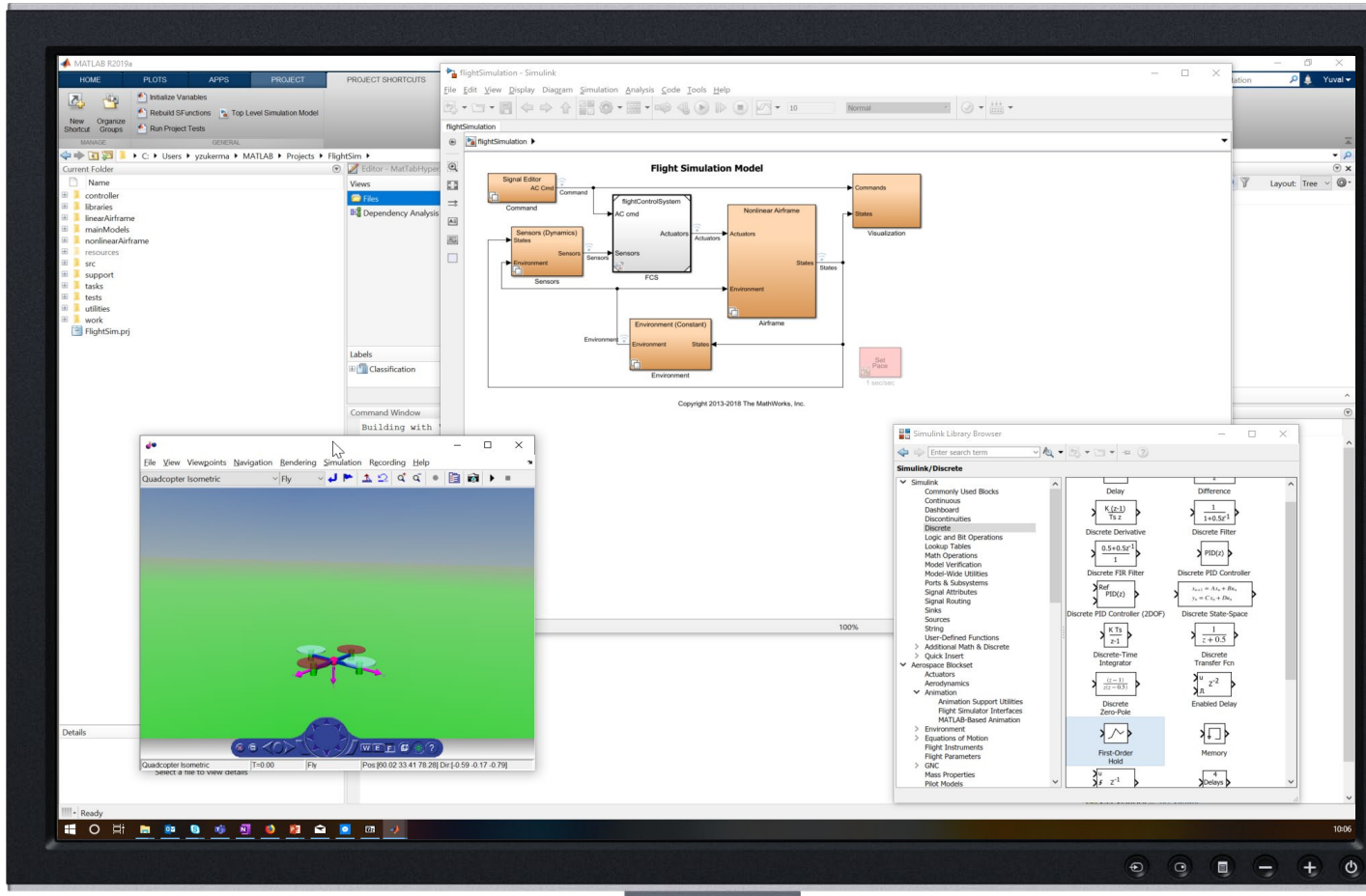
Industry-Specific Solutions

Code Generation

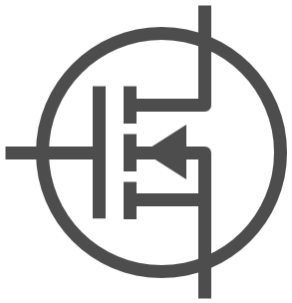
Embedded Systems

Model-Based Design

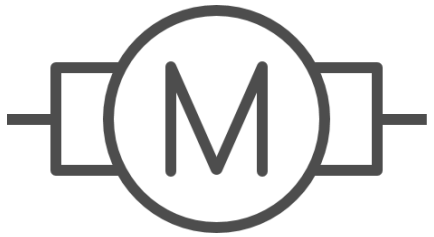
Real-Time Simulation & Testing



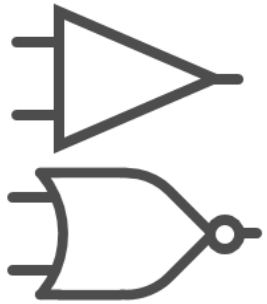
Simscape Electrical & Motor Control Blockset Component Models



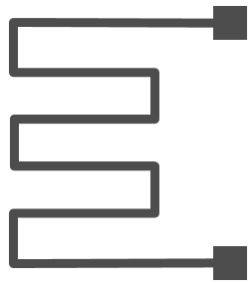
Semi-conductors



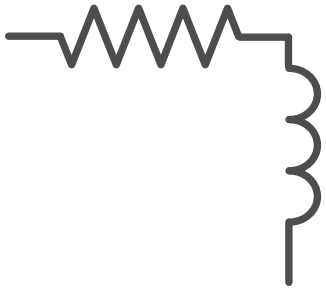
Motors, Actuators



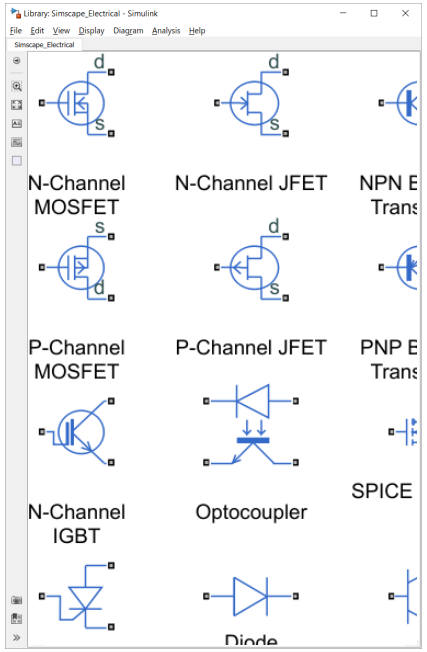
Op-Amps, Logic Gates

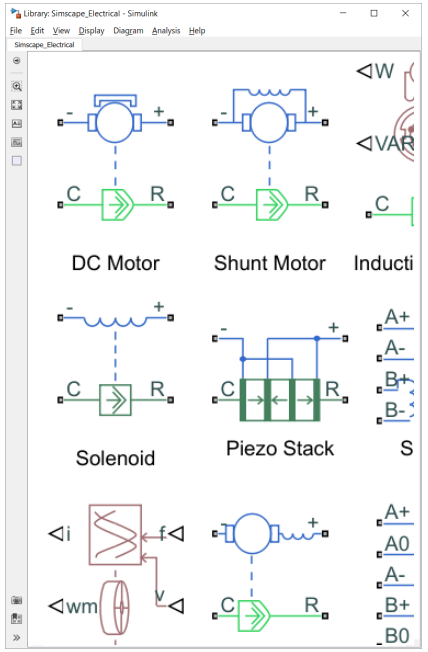


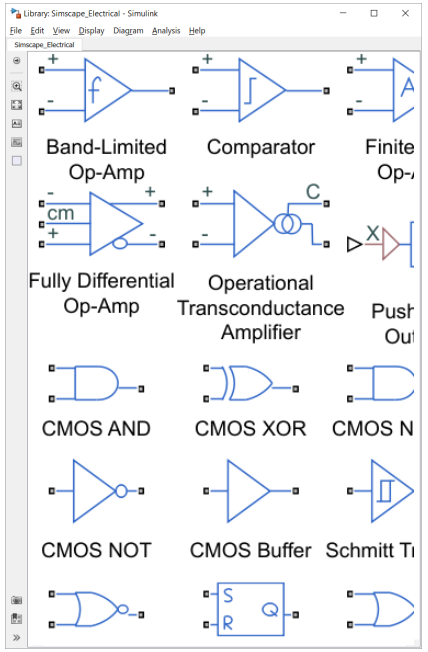
Sensors

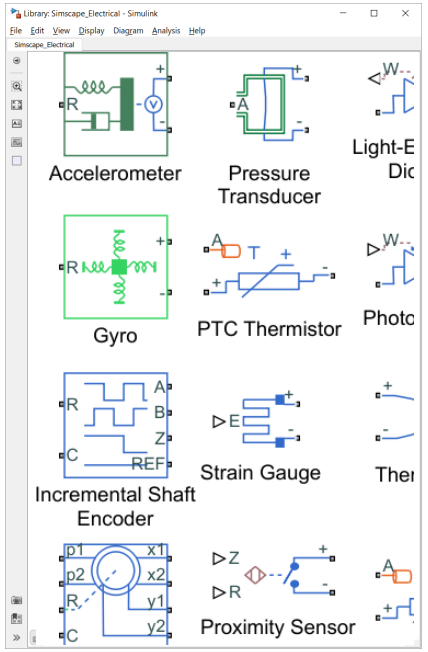


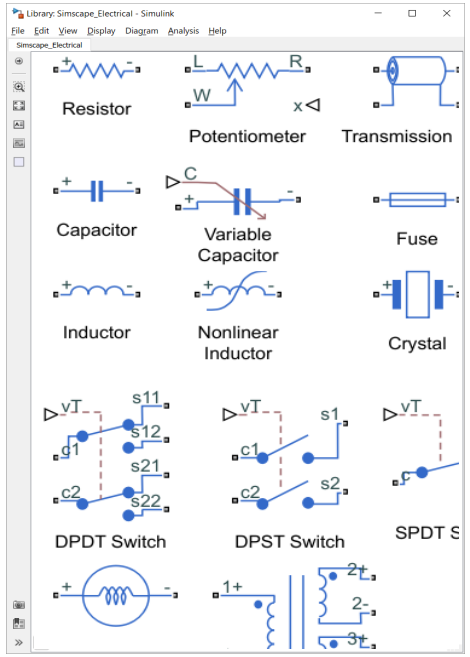
Passive Devices



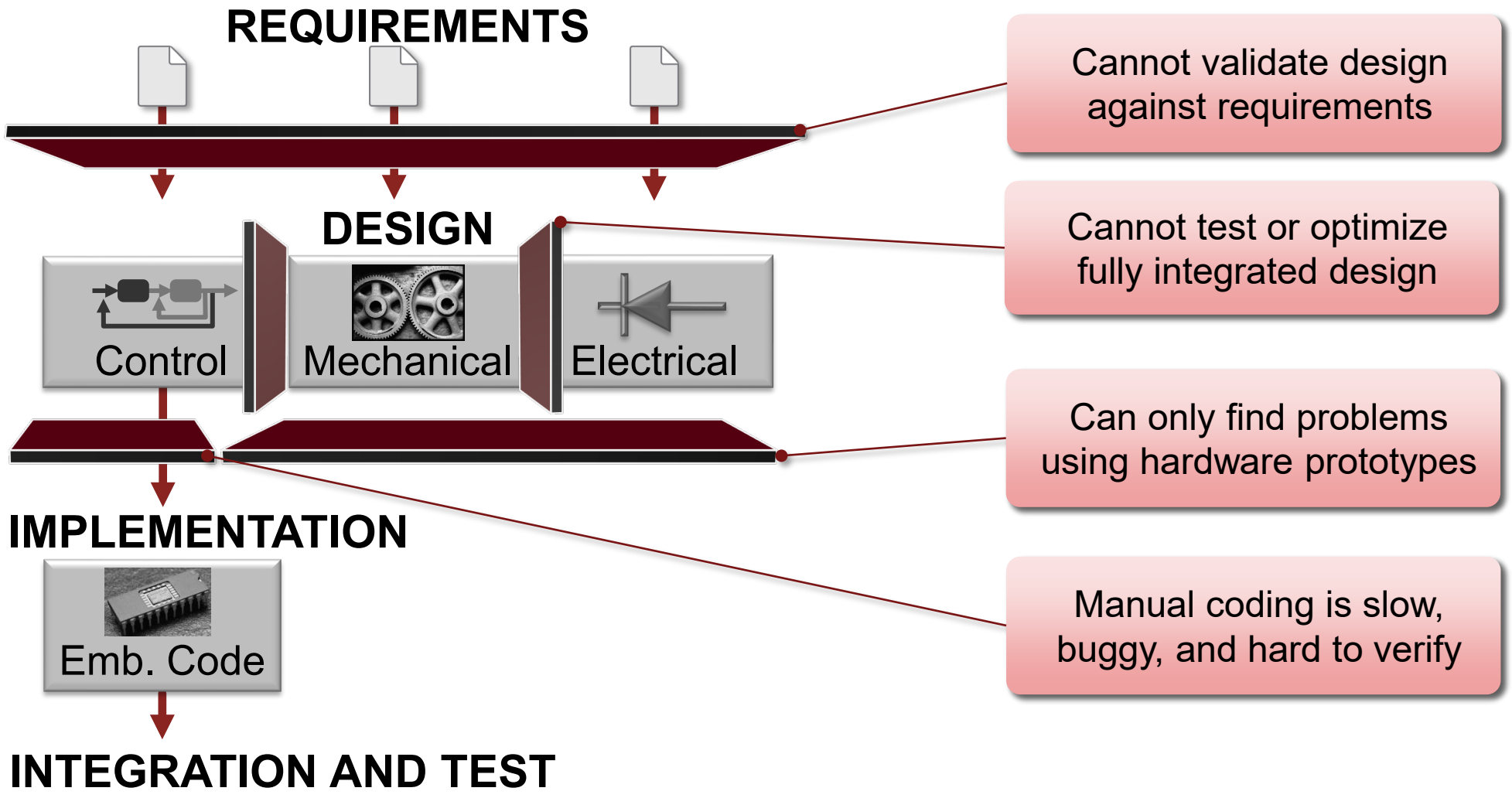




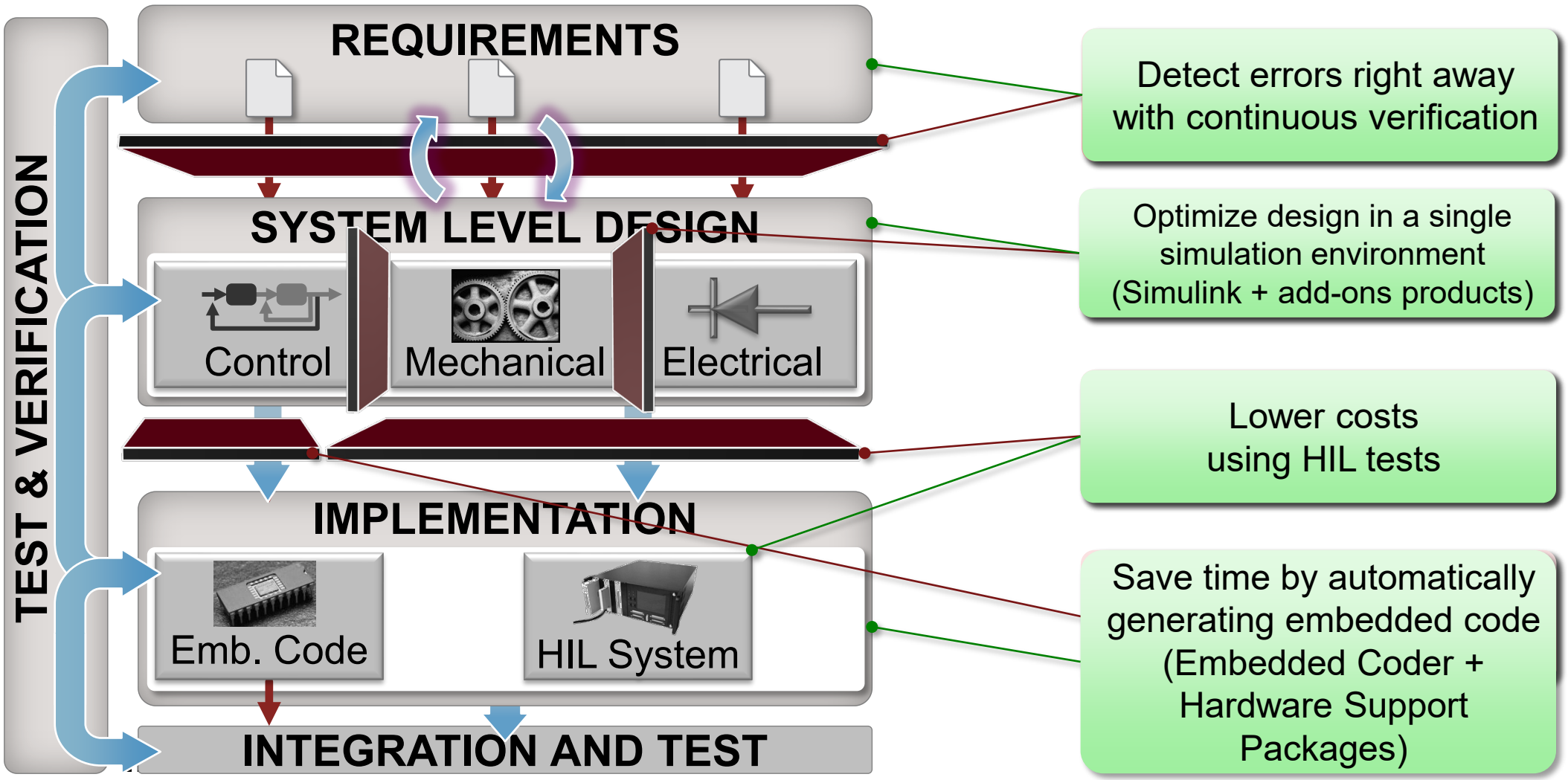




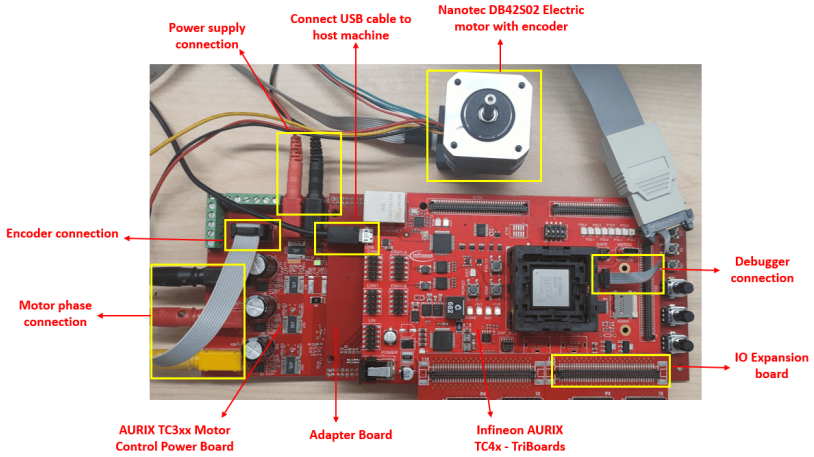
Traditional Design Process

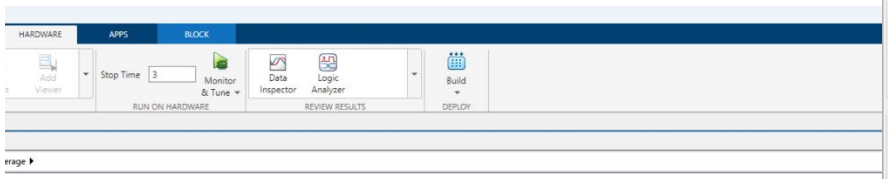


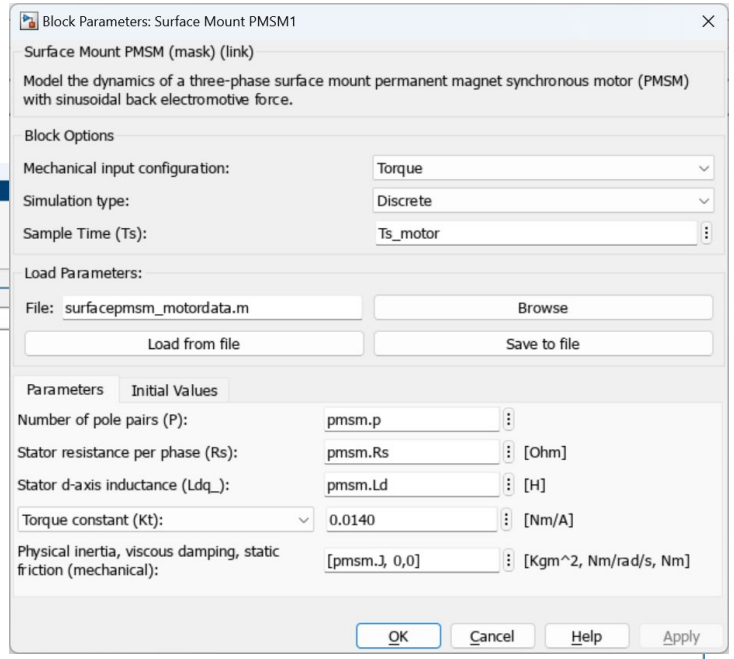
Model-Based Design

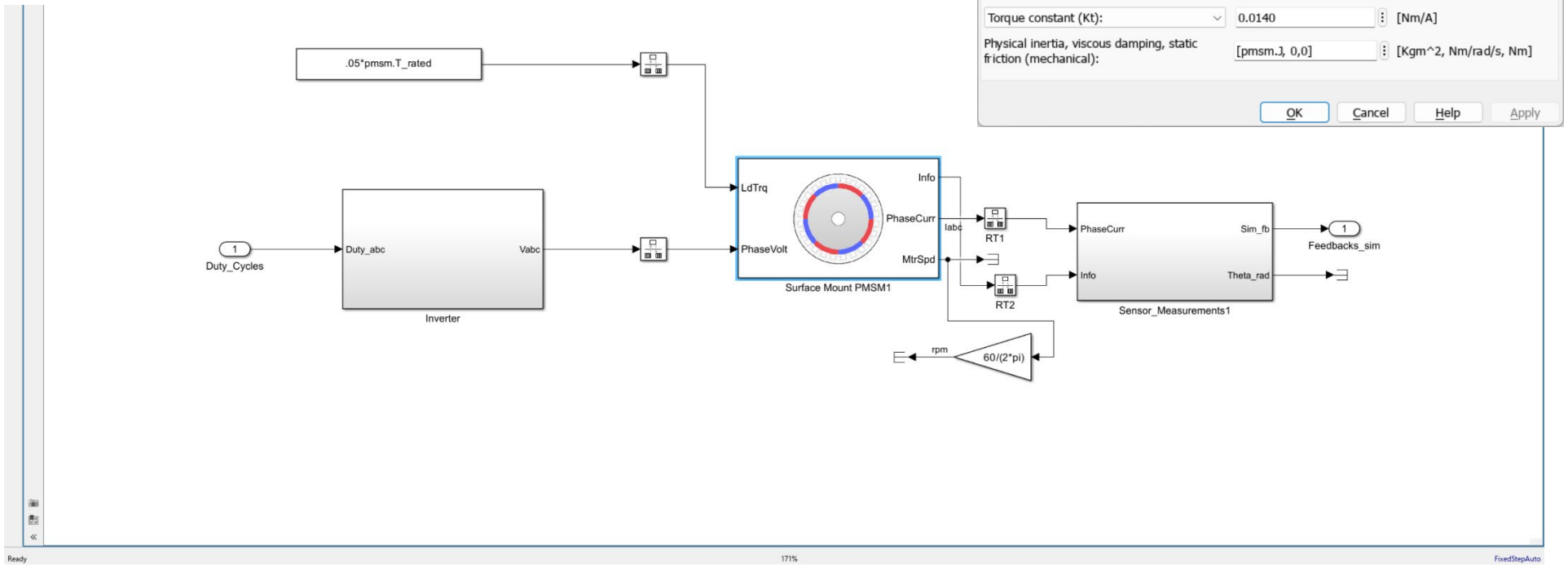


Modeling a Motor Control System

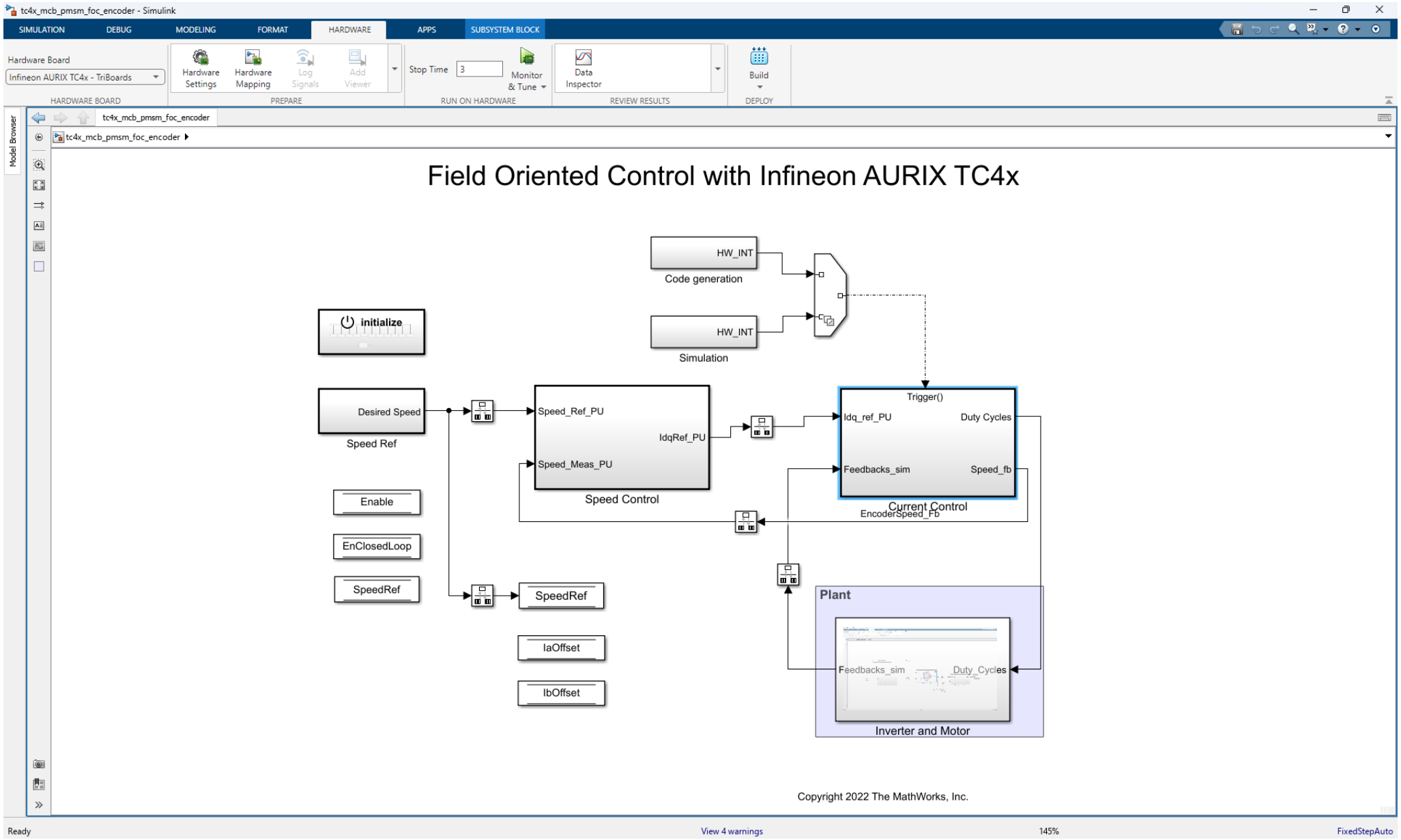




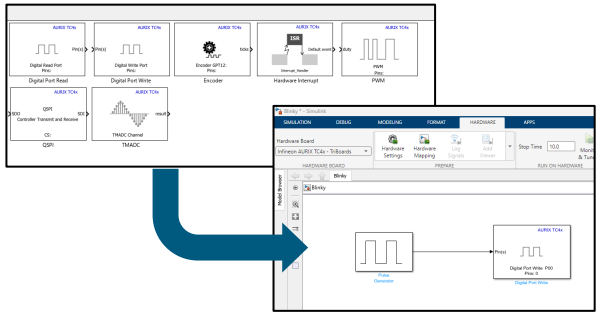




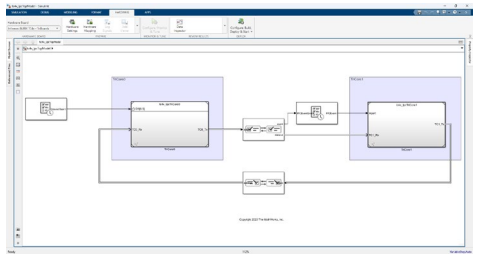
Modeling a Motor Control System



MathWorks Hardware Support Packages enable engineers to rapidly develop on Infineon AURIX™ TC4x without deep device knowledge



Peripheral driver blocks enable hardware peripheral use in deployed Simulink models



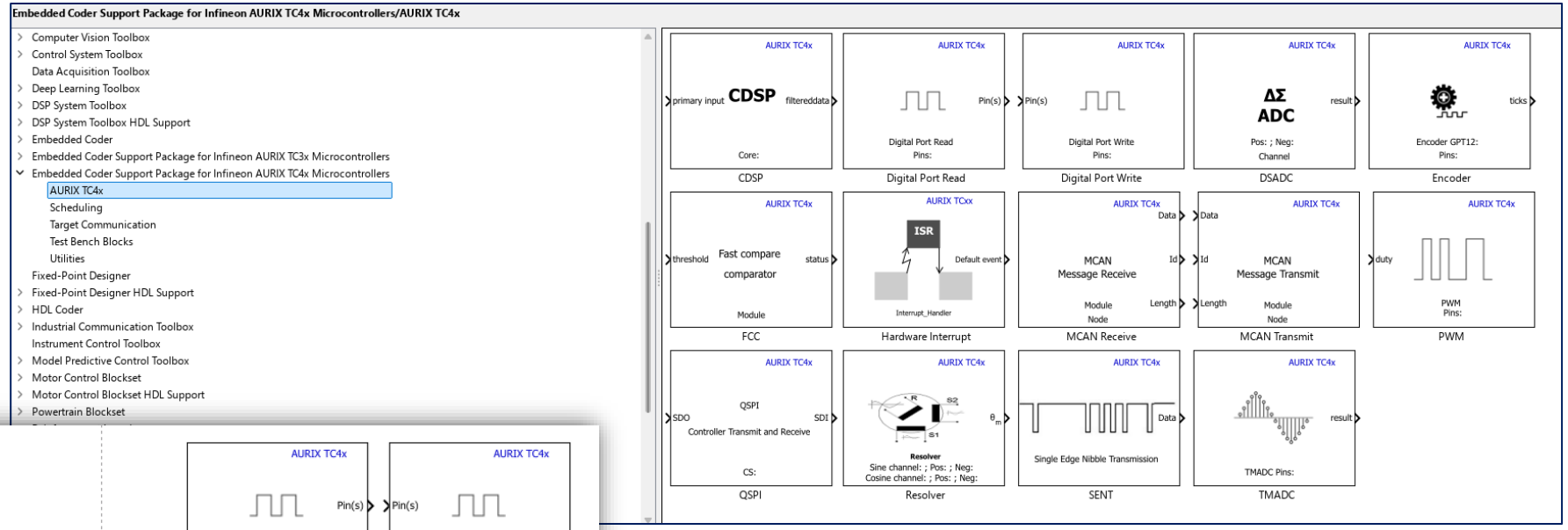
Multi-core model example simulates IPC and then deploys to hardware

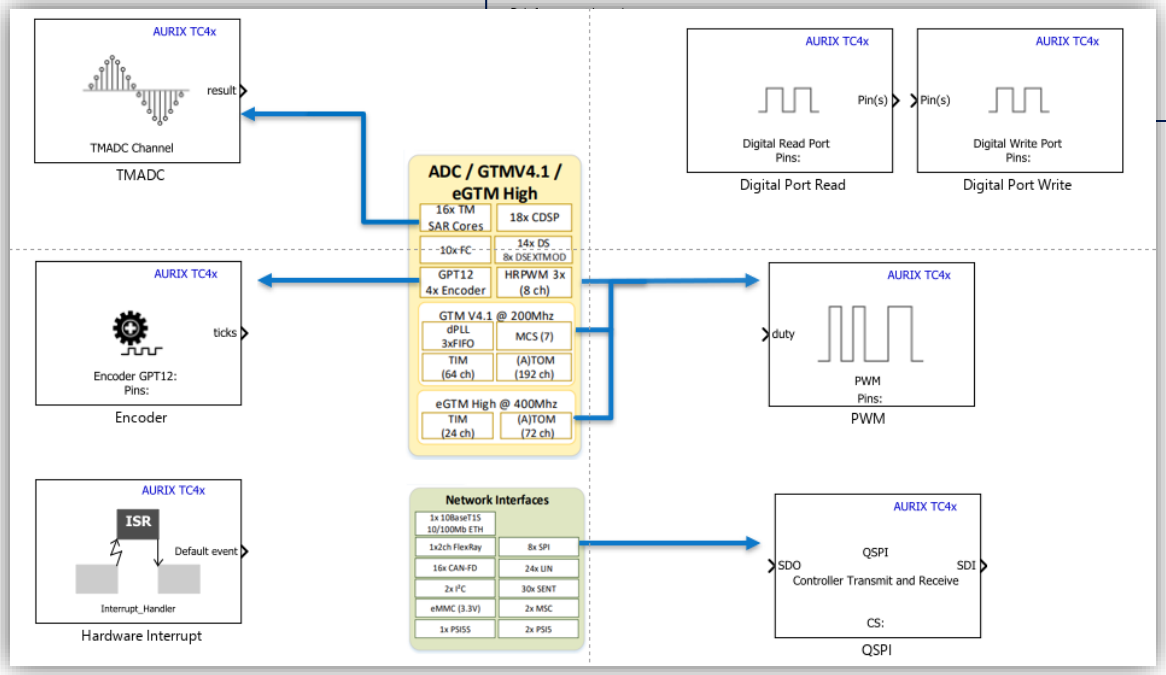
Embedded Coder Support Package for Infineon AURIX TC4x Microcontrollers

Design, simulate and deploy Simulink models on Infineon® AURIX™ TC4x Microcontrollers

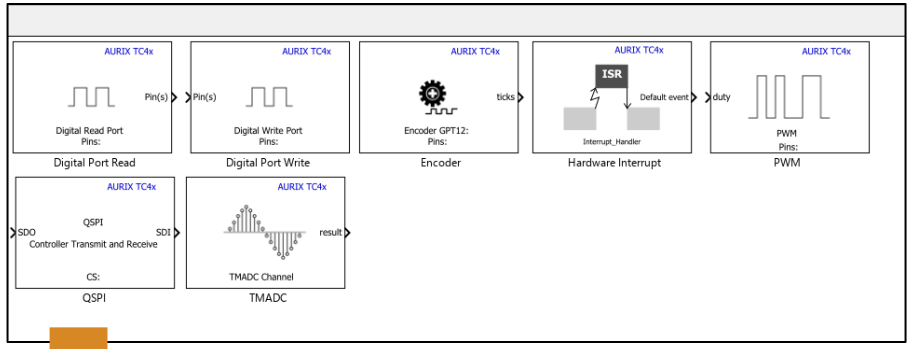
- **Get started with the hardware in minutes**
- Useful for **quick prototyping using peripheral blocks**
- **Includes peripheral driver blocks** and jump start examples (Ex. FOC motor control)
  - TMADC, DSADC, CDSP, FCC, PWM, encoder, resolver, QSPI, SENT, CAN, digital I/O, and hardware interrupt
- Supports TASKING SmartCode, Green Hills® MULTI, Synopsys ARC® MetaWare and HighTec LLVM compilers
- **Generate optimized code for the Vector DSP Accelerator PPU and multiple TriCore™ cores**
- **Facilitating multi-core integration through automatically generated Inter Processor Communication**
- Useful for performing Processor-In-Loop (PIL) tests on TriCore™ and PPU
- Useful for **partitioning algorithms to run on multiple** TriCore™ cores and **PPU**
- Analyze algorithm resource usage and task execution

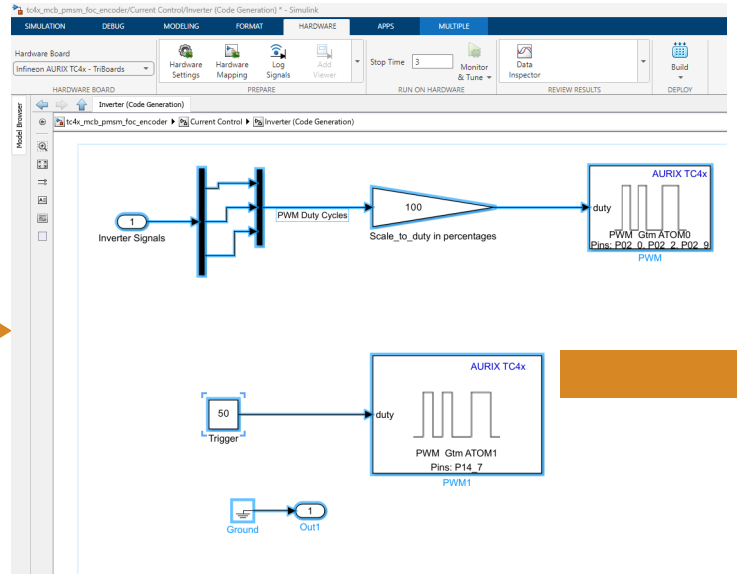
Hardware-specific Peripheral Block Library for Infineon AURIX™ TC4x

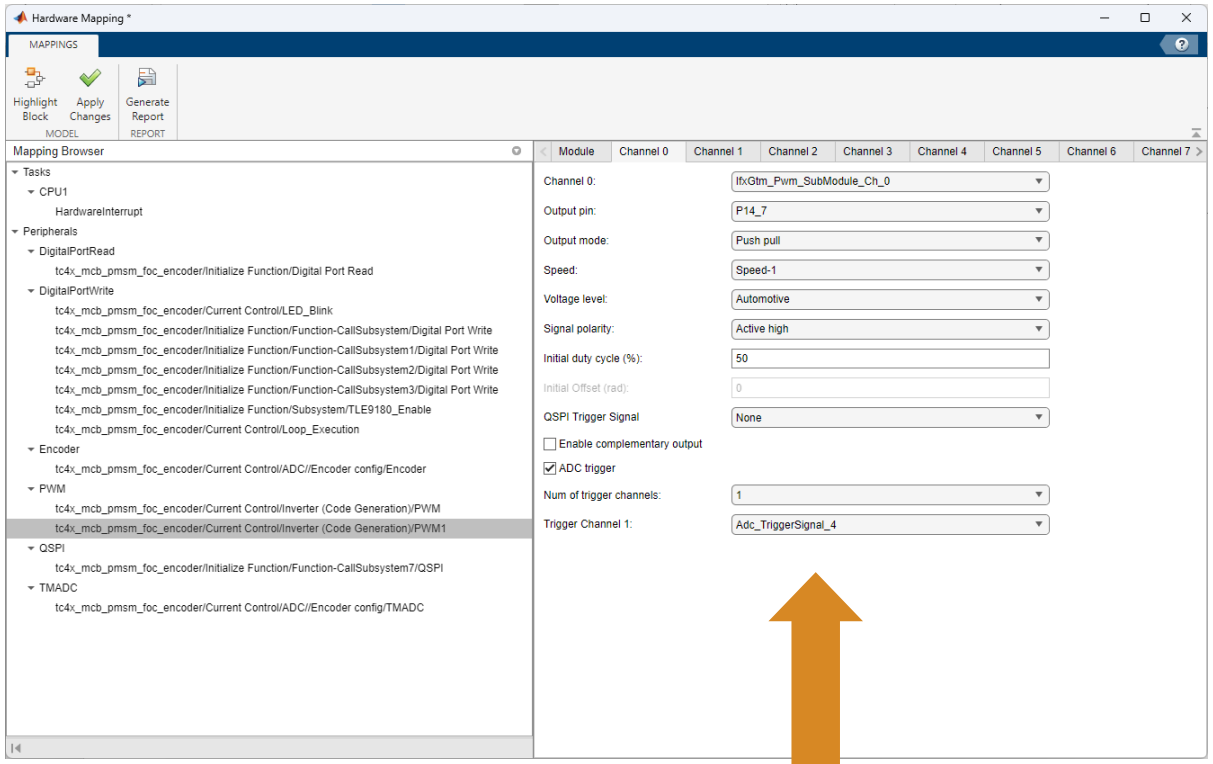




AURIX TC4x Peripheral Blocks for Code Generation



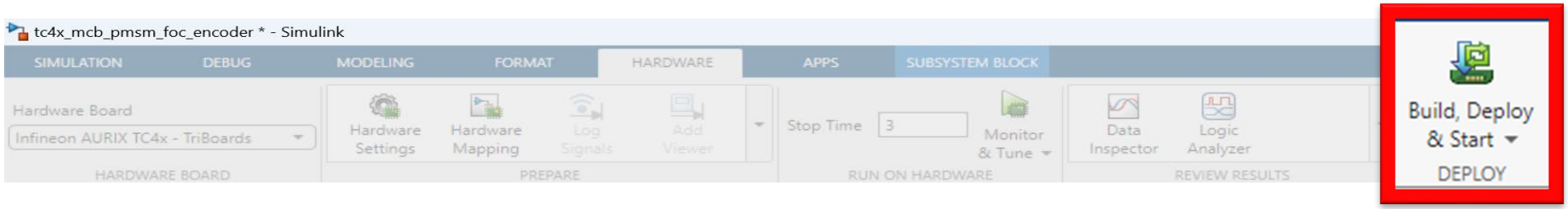




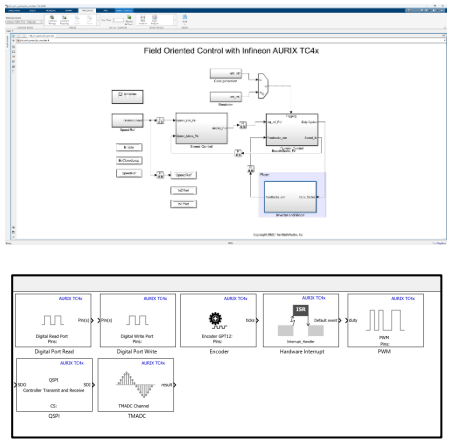
Drag and drop Simulink and Infineon AURIX Peripheral Blocks

Configure Infineon AURIX Peripheral Blocks using Hardware Mapping

Build, Deploy & Start



Simulink Model



AURIX HSP + Embedded Coder

Compiler

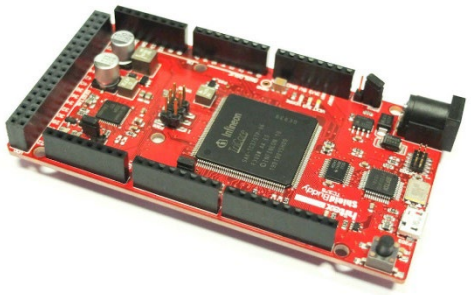
TASKING

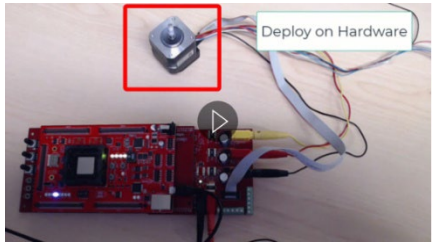
HIGHTEC

Green Hills SOFTWARE

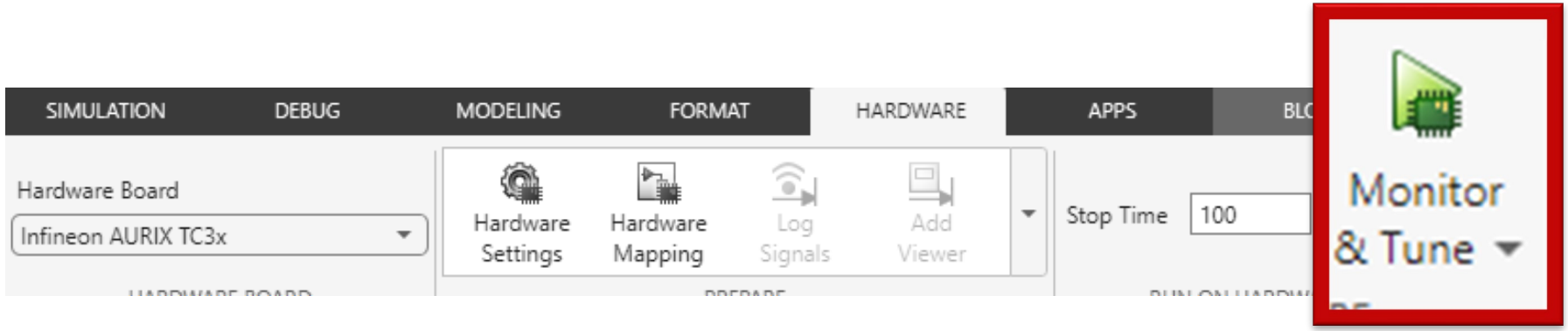
SYNOPSYS

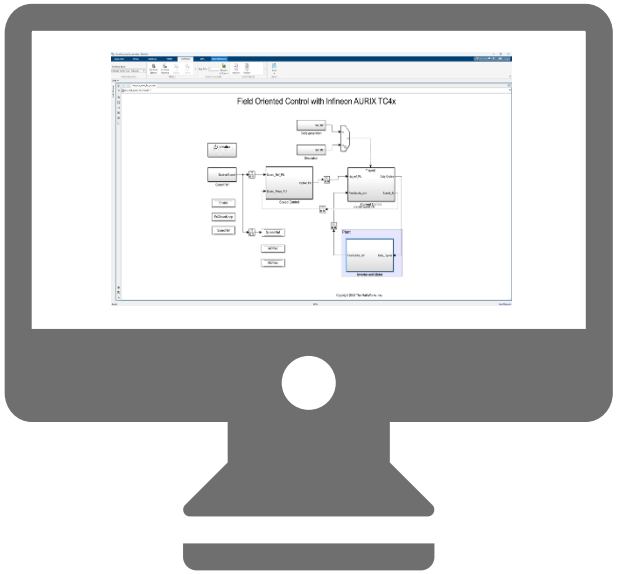
Run on AURIX



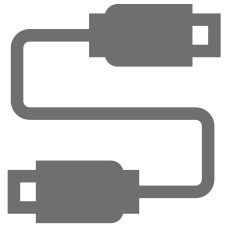


Debugging using Monitor and tune: Log signal data and tune parameters

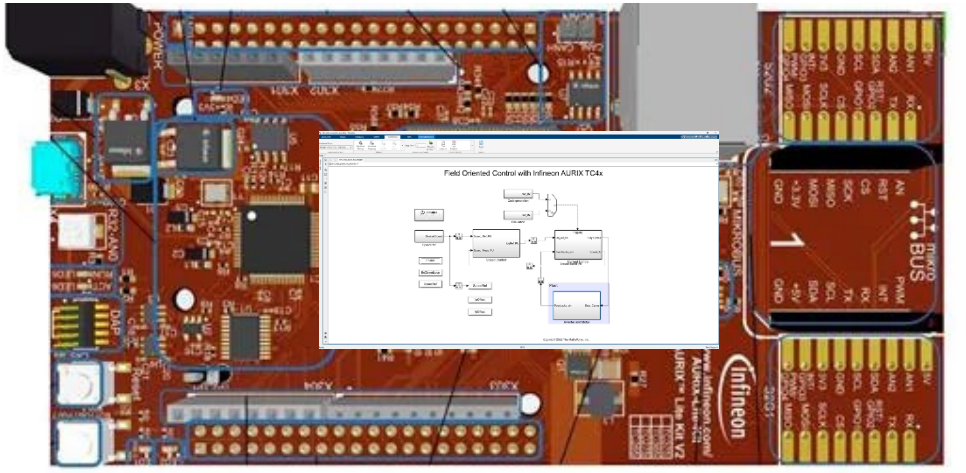




Simulink Model

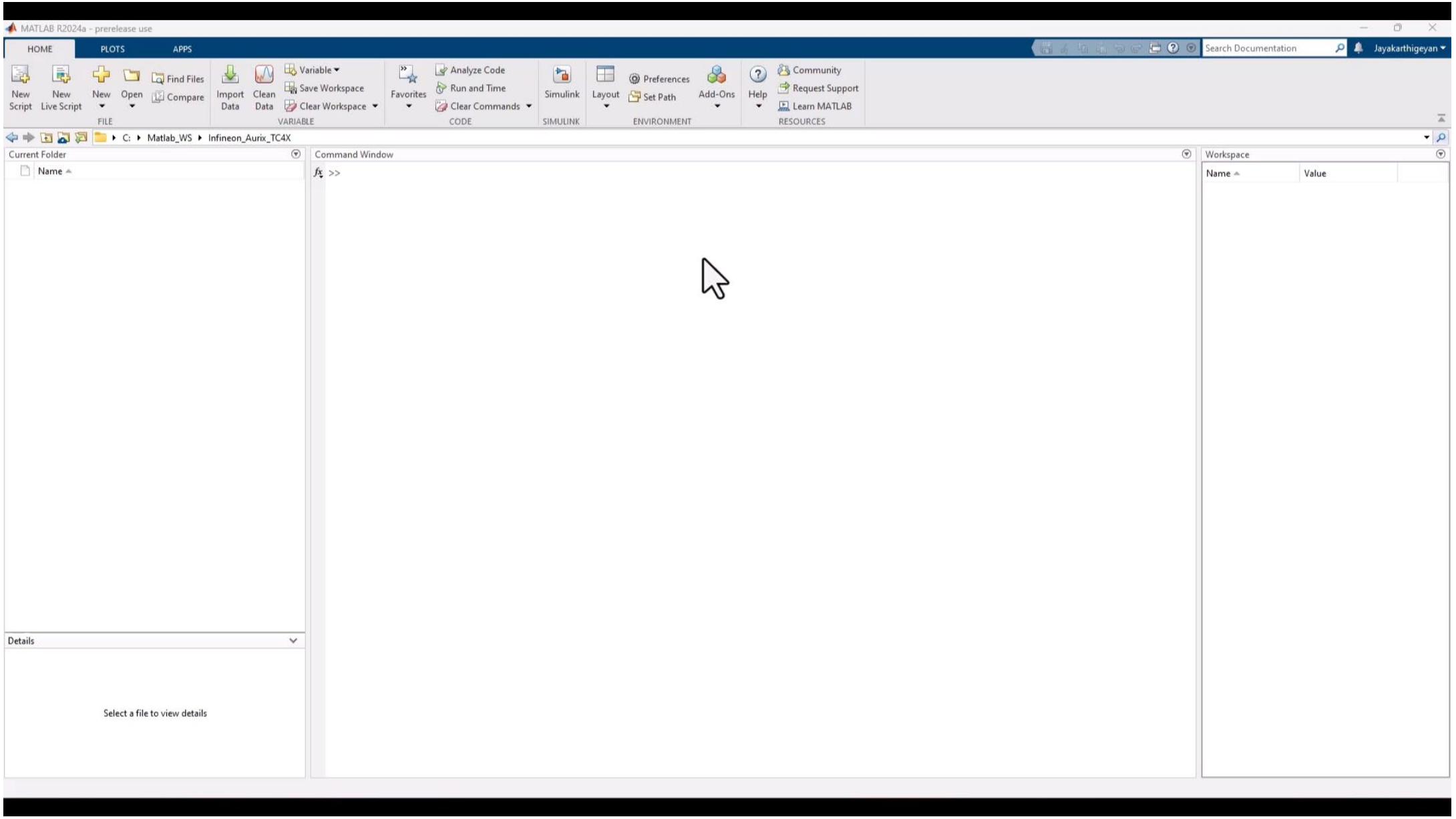


Data Exchange over Serial

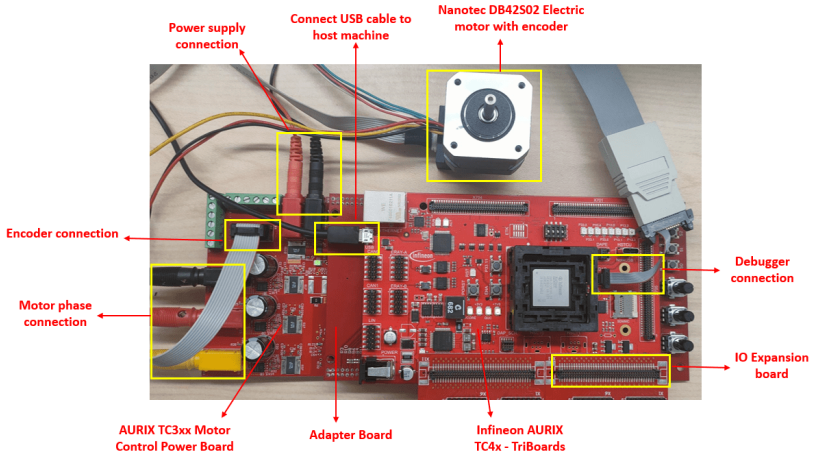


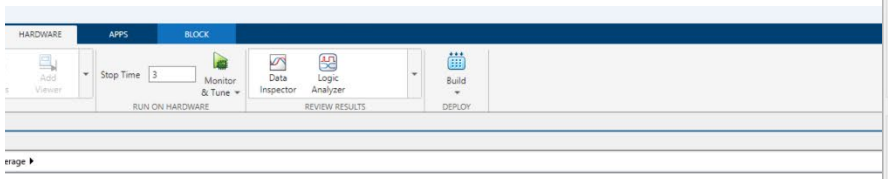
Model running on hardware with additional code to monitor and tune parameters on Simulink

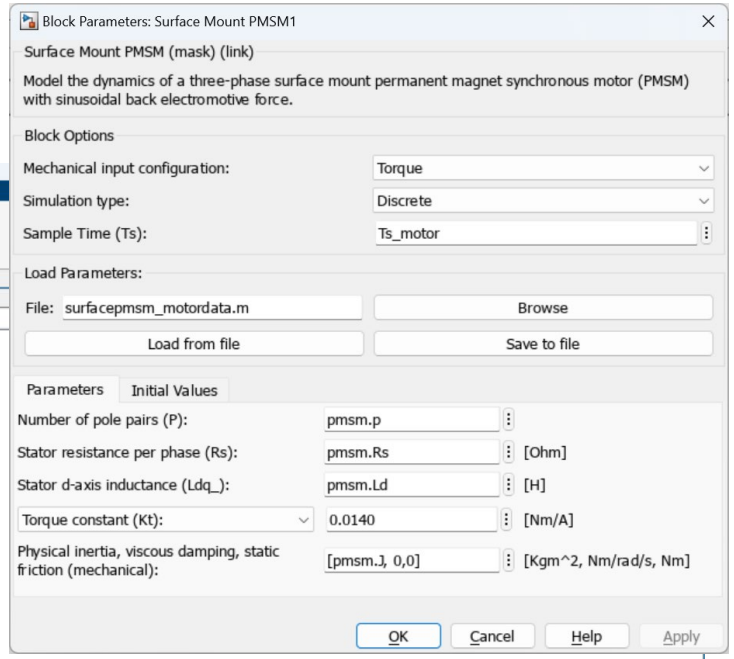
Getting Started in Minutes: Deploy, Monitor and Tune

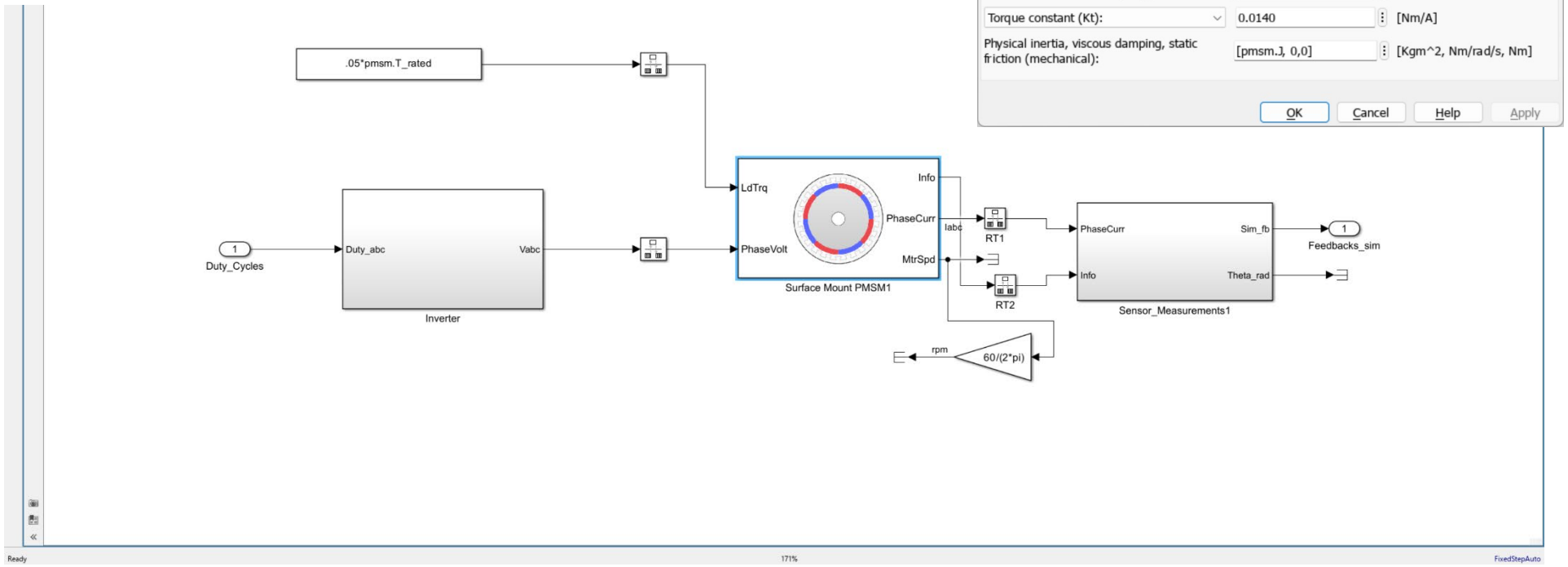


Modeling a Motor Control System

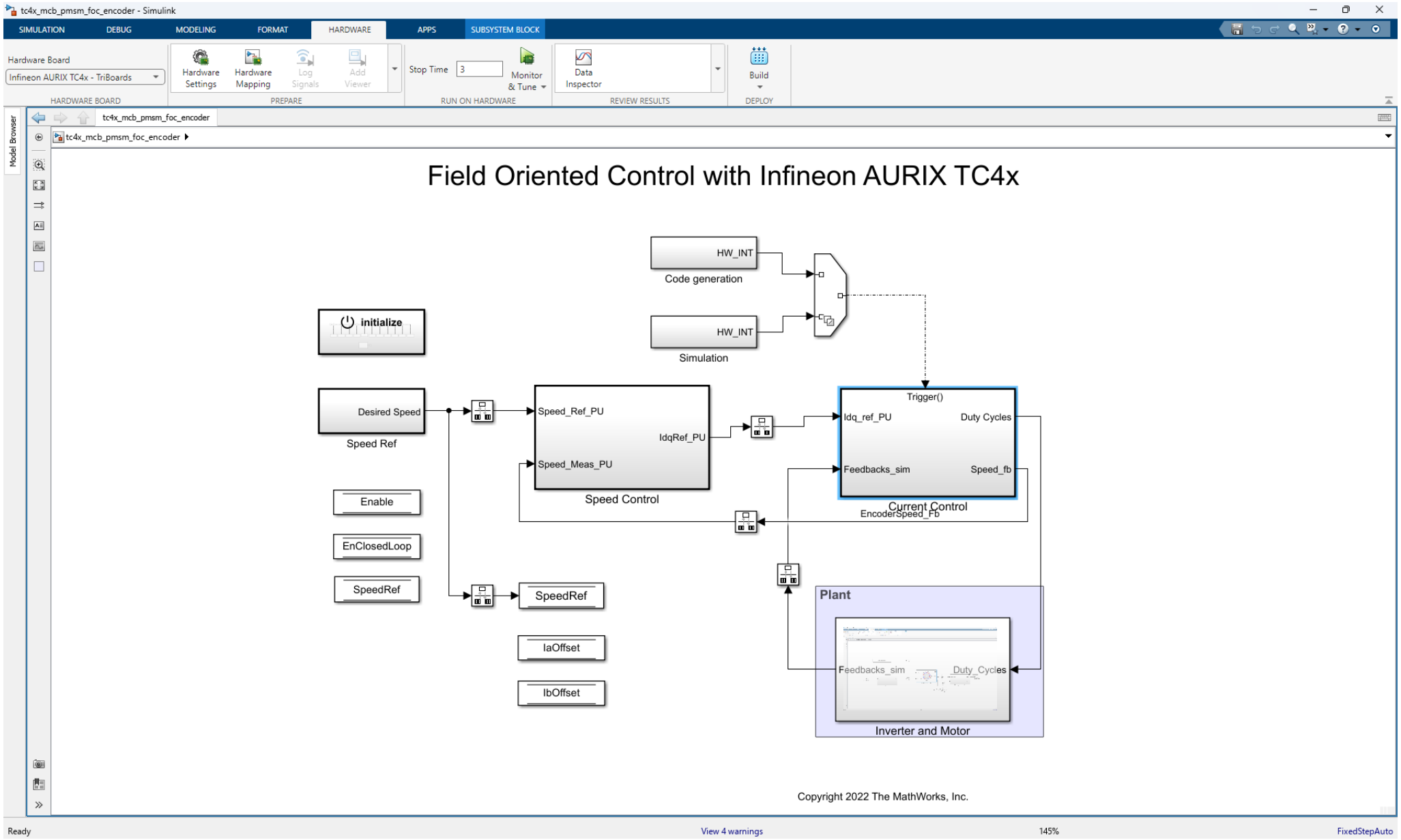


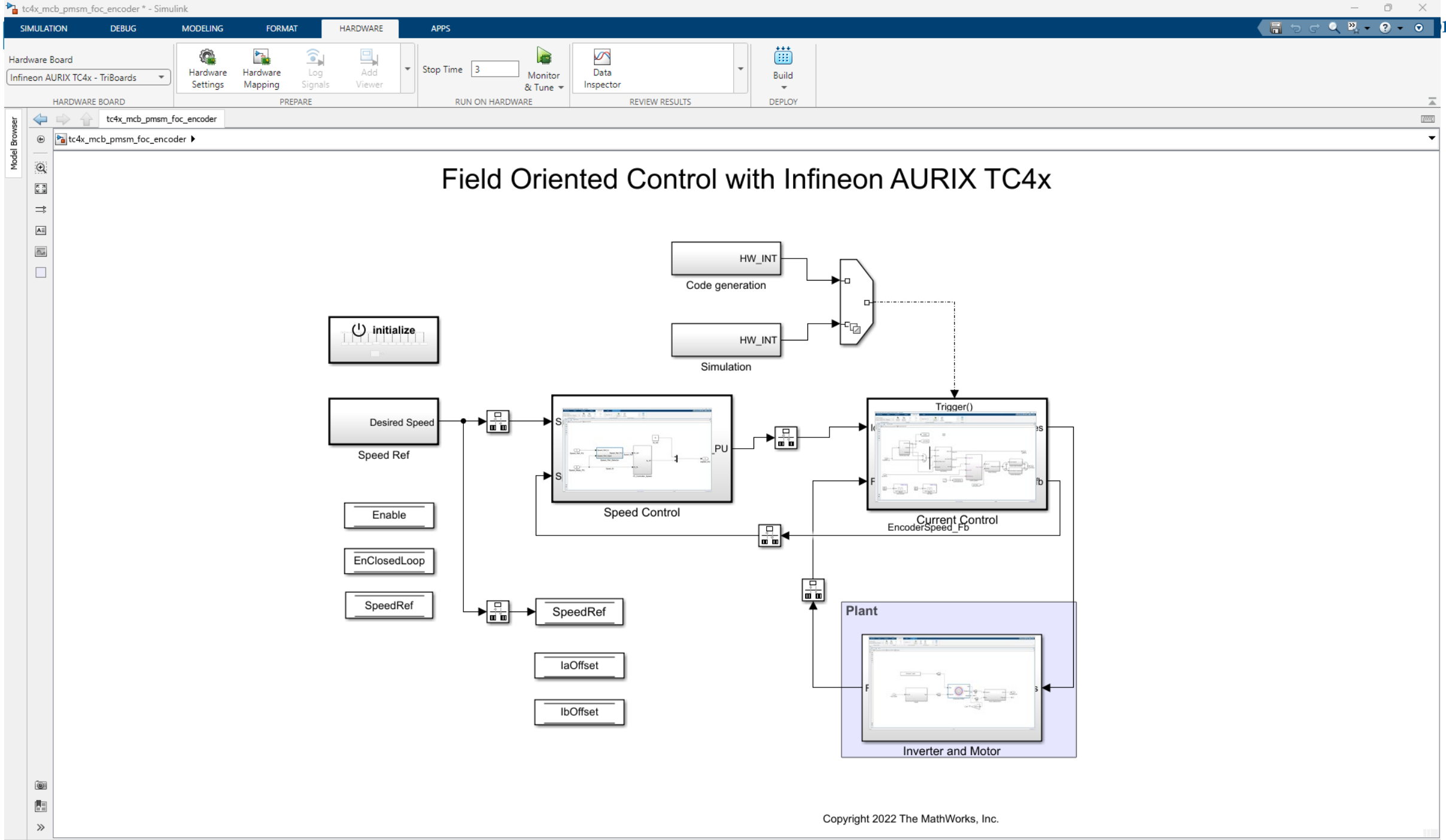


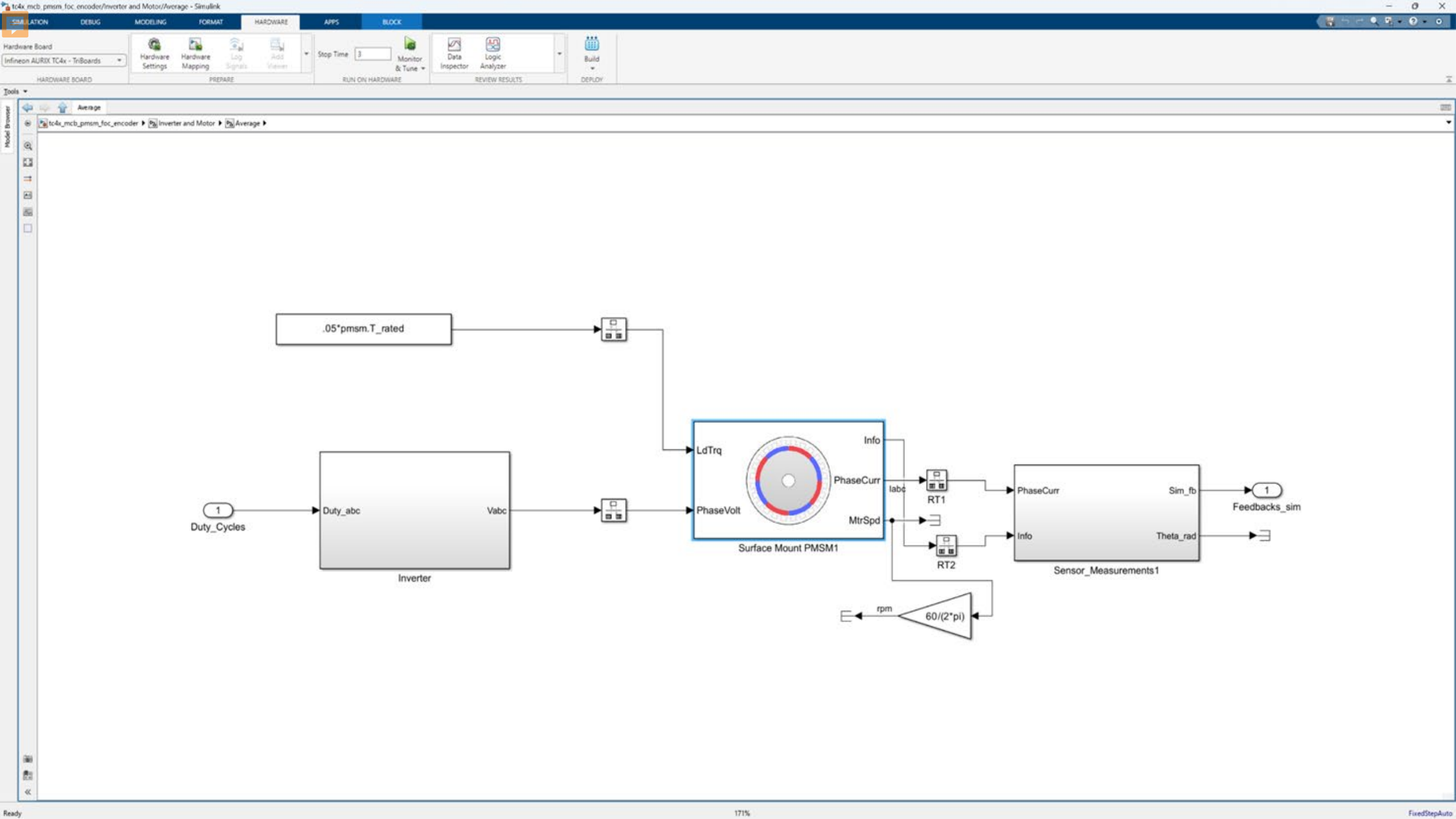




Modeling a Motor Control System




tc4x_mcb_pmsm_foc_encoder * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
Hardware Board
Infineon AURIX TC4x - TriBoards
HARDWARE BOARD
Hardware Settings
Hardware Mapping
Log Signals
Add Viewer
PREPARE
Stop Time
3
Monitor & Tune
RUN ON HARDWARE
Data Inspector
REVIEW RESULTS
Build
DEPLOY
Model Browser
tc4x_mcb_pmsm_foc_encoder
Field Oriented Control with Infineon AURIX TC4x
HW_INT
Code generation
HW_INT
Simulation
initialize
Desired Speed
Speed Ref
Enable
EnClosedLoop
SpeedRef
SpeedRef
IaOffset
IbOffset
Speed Control
Trigger()
Current Control
EncoderSpeed_Fb
Plant
Inverter and Motor
Copyright 2022 The MathWorks, Inc.
Ready
View 4 warnings
145%
FixedStepAuto


tc4x_mcb_pmsm_foc_encoder/Inverter and Motor/Average - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
BLOCK
Hardware Board
Infineon AURIX TC4x - TriBoards
HARDWARE BOARD
Hardware Settings
Hardware Mapping
Log Signals
Add Viewer
PREPARE
Stop Time
3
Monitor & Tune
RUN ON HARDWARE
Data Inspector
Logic Analyzer
REVIEW RESULTS
Build
DEPLOY
Tools
Model Browser
Average
tc4x_mcb_pmsm_foc_encoder
Inverter and Motor
Average
.05*pmsm.T_rated
1
Duty_Cycles
Duty_abc
Vabc
Inverter
LdTrq
PhaseVolt
Info
PhaseCurr
MtrSpd
Surface Mount PMSM1
Iabc
RT1
RT2
PhaseCurr
Info
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Theta_rad
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Feedbacks_sim
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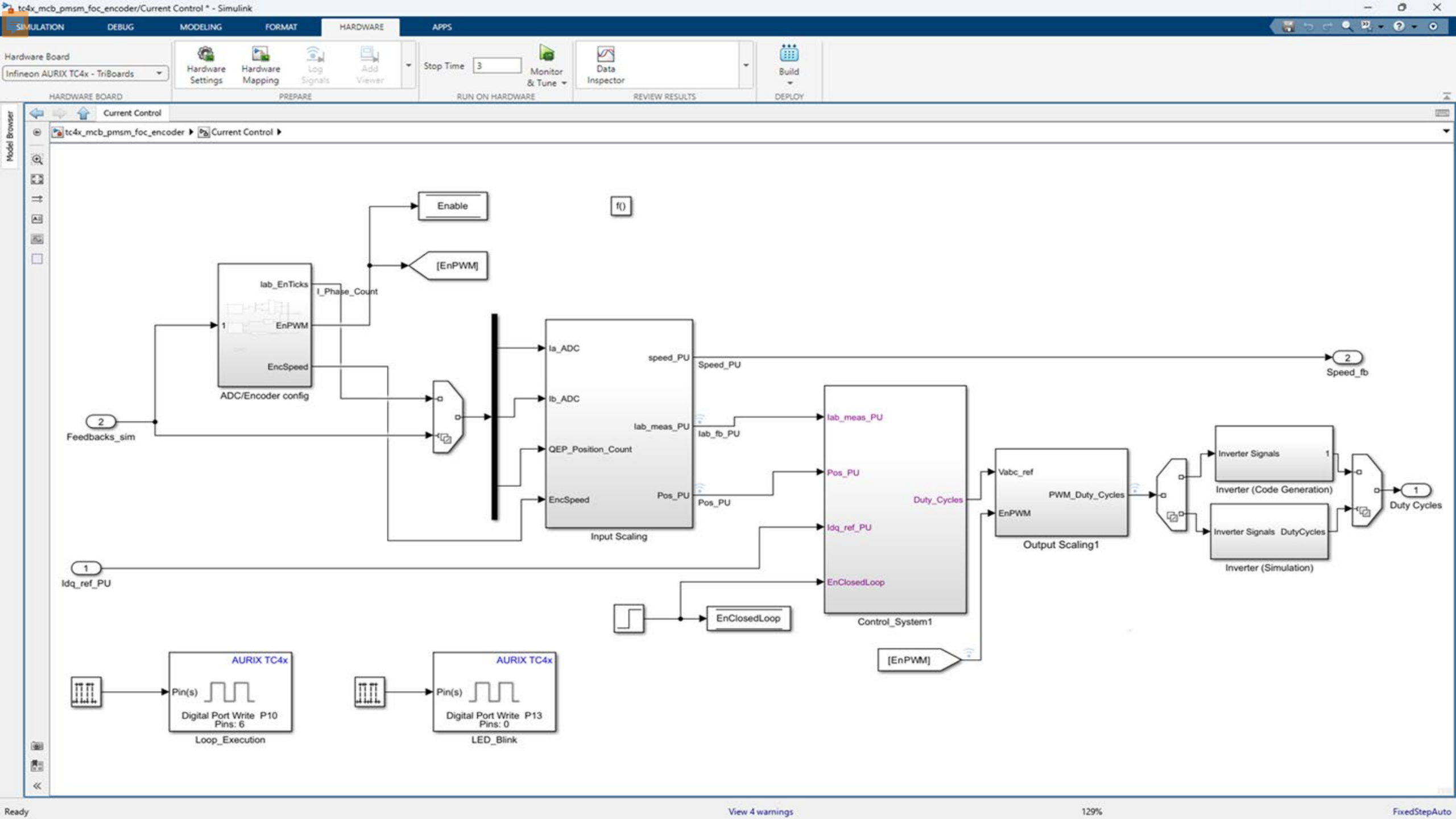
tc4x_mcb_pmsm_foc_encoder/Current Control * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
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Infineon AURIX TC4x - TriBoards
HARDWARE BOARD
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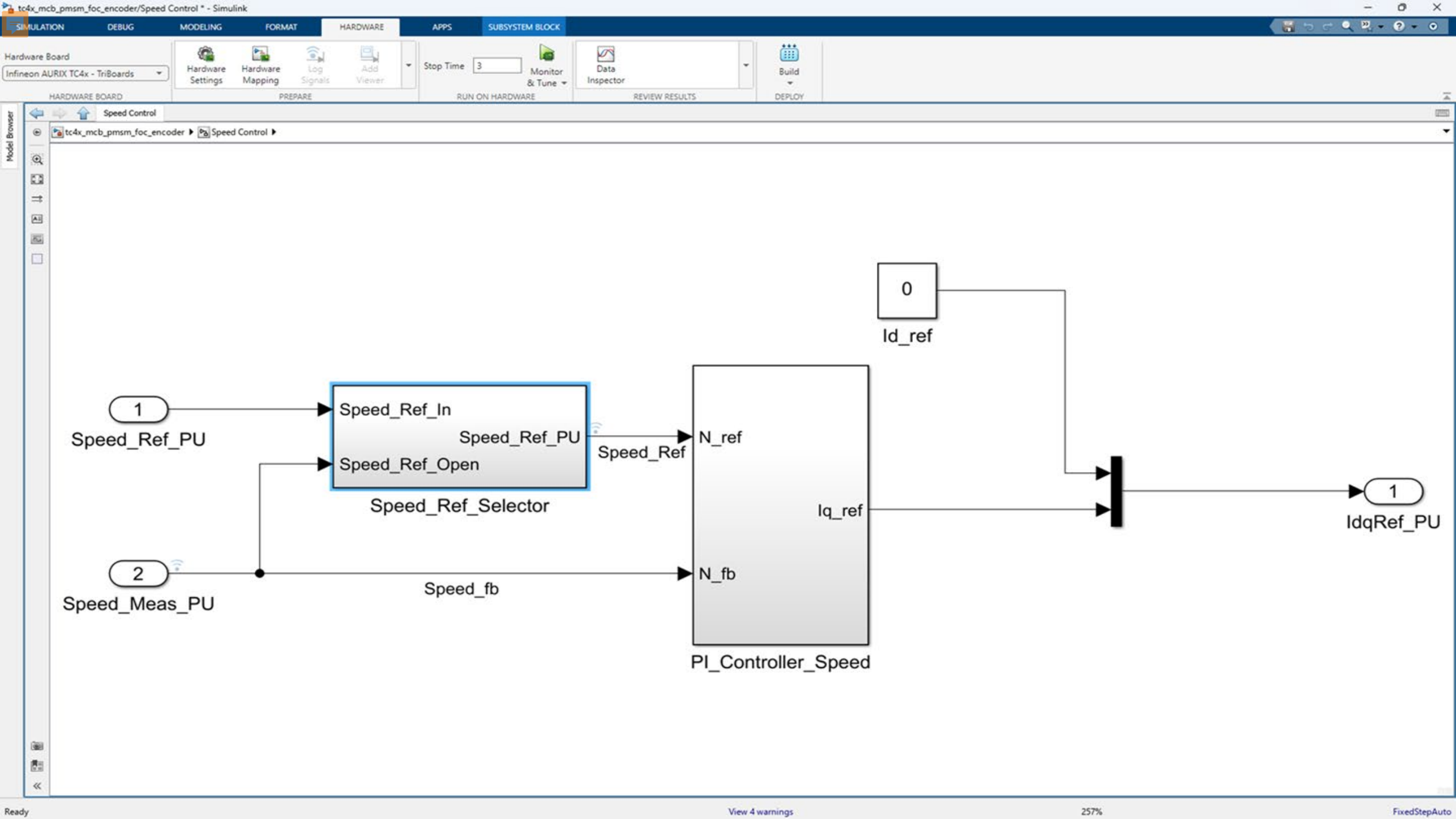
DEPLOY
Model Browser
Current Control
tc4x_mcb_pmsm_foc_encoder
Current Control
Enable
f()
[EnPWM]
Iab_EnTicks
I_Phase_Count
1
EnPWM
EncSpeed
ADC/Encoder config
2
Feedbacks_sim
Ia_ADC
Ib_ADC
QEP_Position_Count
EncSpeed
speed_PU
lab_meas_PU
Pos_PU
Input Scaling
Speed_PU
2
Speed_fb
lab_fb_PU
Pos_PU
lab_meas_PU
Pos_PU
Idq_ref_PU
EnClosedLoop
Duty_Cycles
Control_System1
1
Idq_ref_PU
EnClosedLoop
Vabc_ref
EnPWM
PWM_Duty_Cycles
Output Scaling1
Inverter Signals
1
Inverter (Code Generation)
Inverter Signals DutyCycles
Inverter (Simulation)
1
Duty Cycles
[EnPWM]
AURIX TC4x
Pin(s)
Digital Port Write P10
Pins: 6
Loop_Execution
AURIX TC4x
Pin(s)
Digital Port Write P13
Pins: 0
LED_Blink
Ready
View 4 warnings
129%
FixedStepAuto


tc4x_mcb_pmsm_foc_encoder/Speed Control * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
SUBSYSTEM BLOCK
Hardware Board
Infineon AURIX TC4x - TriBoards
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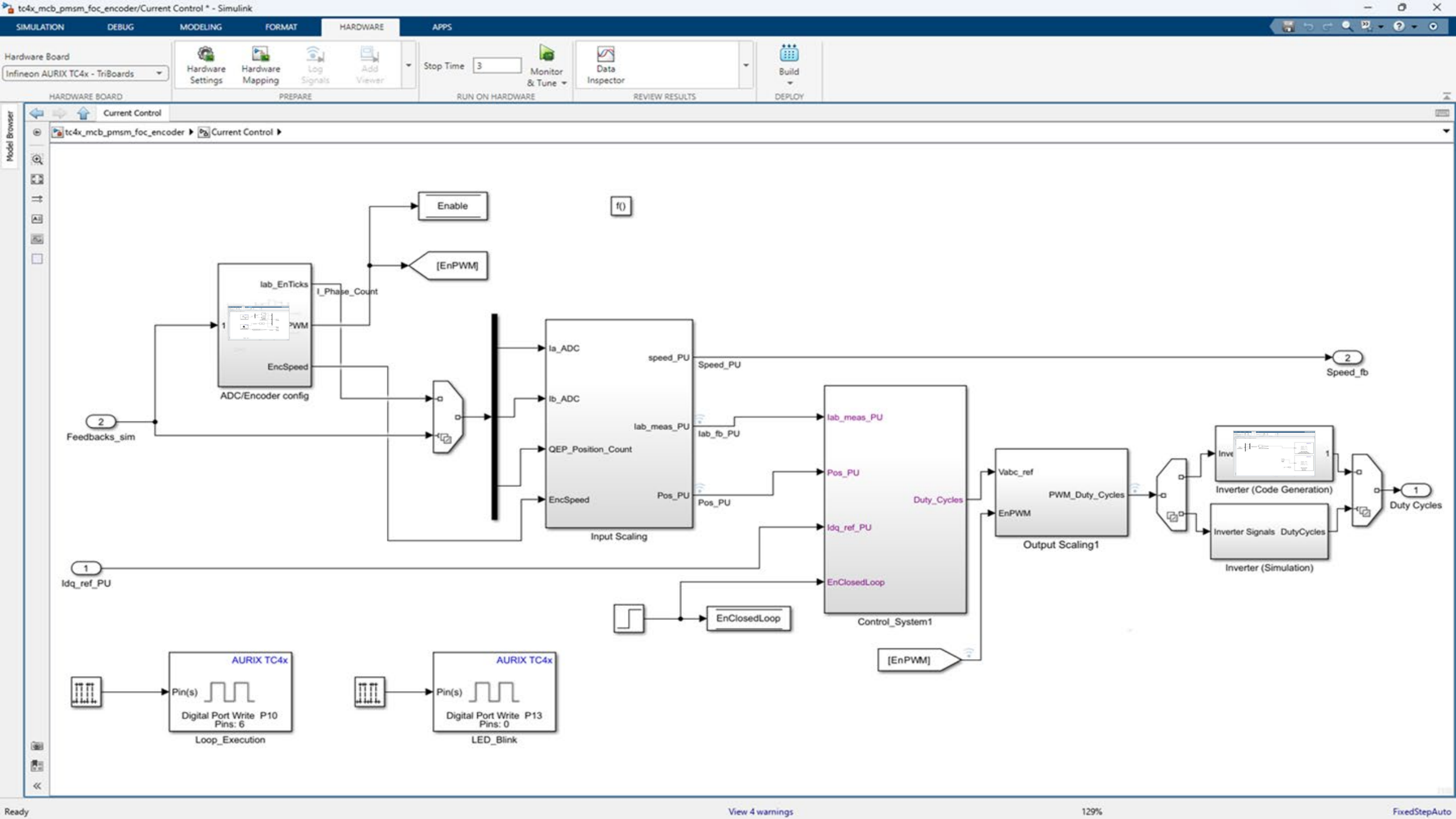
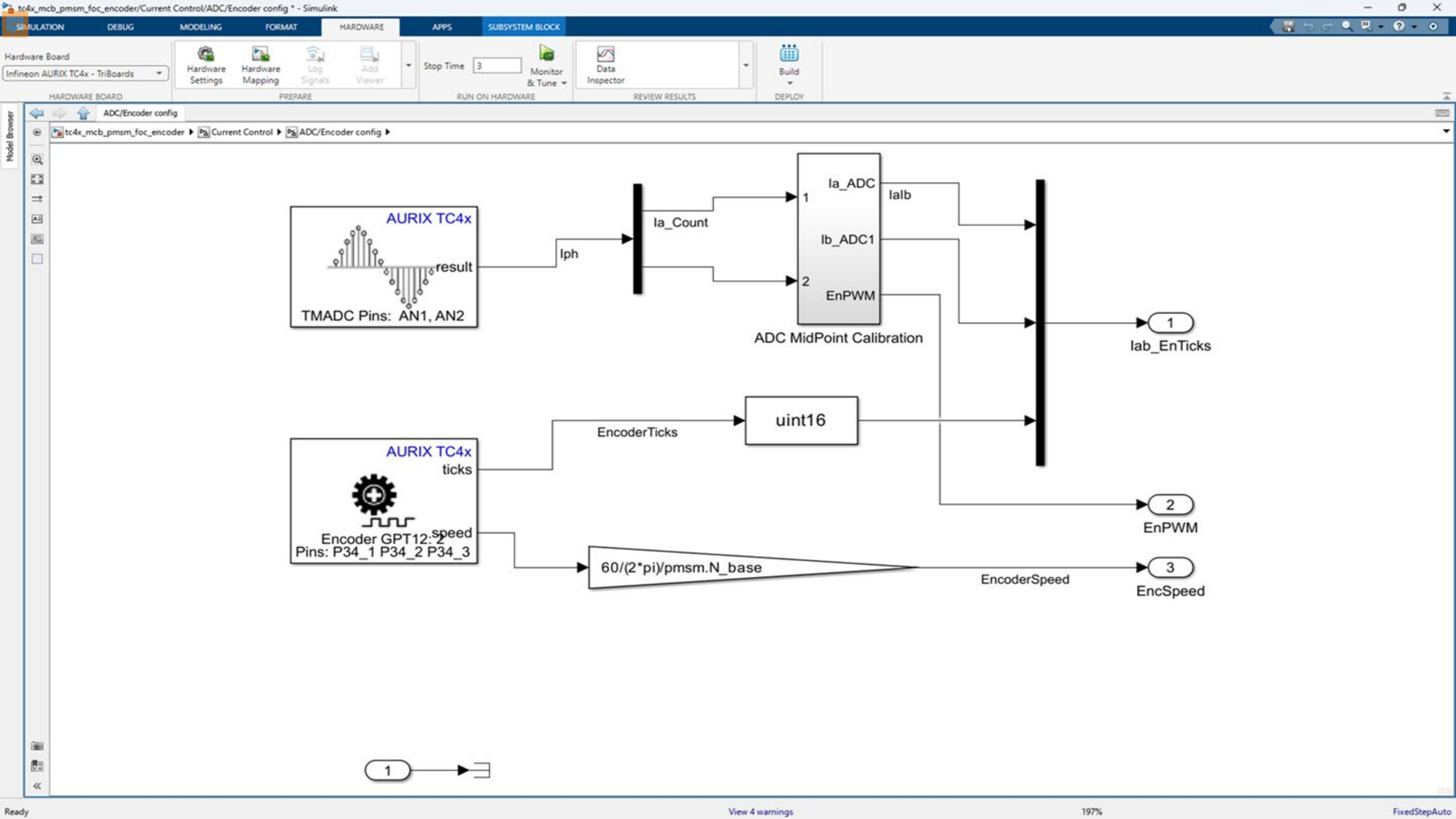
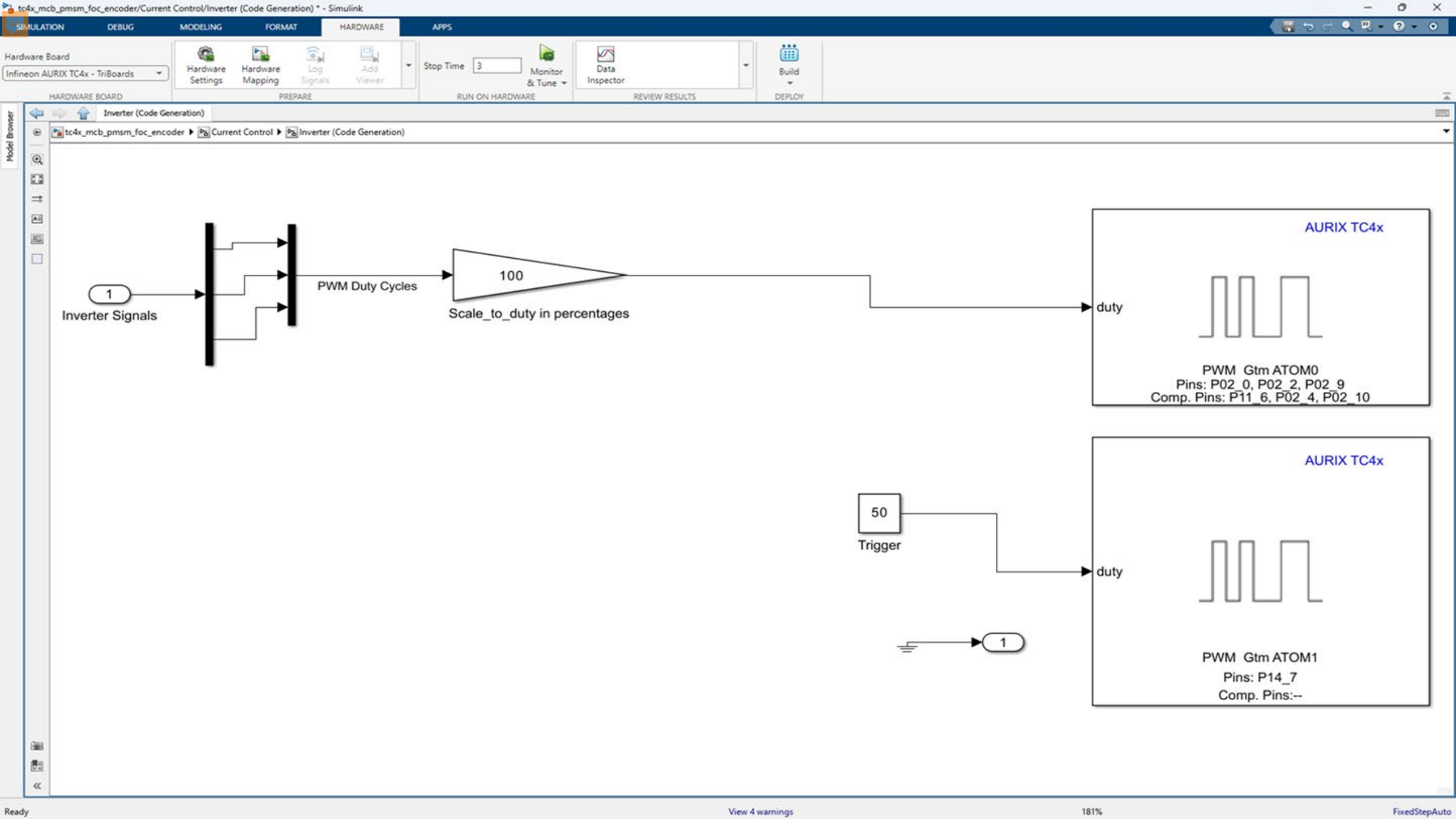
DEPLOY
Model Browser
Speed Control
tc4x_mcb_pmsm_foc_encoder
Speed Control
0
Id_ref
1
Speed_Ref_PU
Speed_Ref_In
Speed_Ref_PU
Speed_Ref_Open
Speed_Ref_Selector
Speed_Ref
N_ref
Iq_ref
N_fb
PI_Controller_Speed
2
Speed_Meas_PU
Speed_fb
1
IdqRef_PU
Ready
View 4 warnings
257%
FixedStepAuto

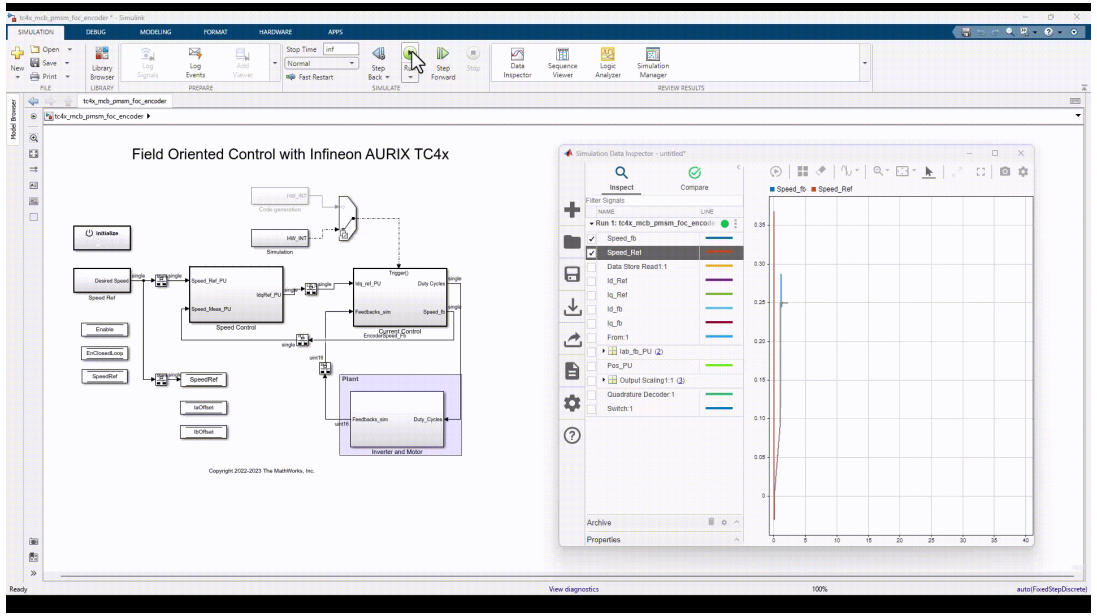

tc4x_mcb_pmsm_foc_encoder/Current Control * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
Hardware Board
Infineon AURIX TC4x - TriBoards
HARDWARE BOARD
Hardware Settings
Hardware Mapping
Log Signals
Add Viewer
PREPARE
Stop Time
3
Monitor & Tune
RUN ON HARDWARE
Data Inspector
REVIEW RESULTS
Build
DEPLOY
Model Browser
Current Control
tc4x_mcb_pmsm_foc_encoder
Current Control
Enable
f()
[EnPWM]
Iab_EnTicks
I_Phase_Count
PWM
EncSpeed
ADC/Encoder config
2
Feedbacks_sim
Ia_ADC
Ib_ADC
QEP_Position_Count
EncSpeed
speed_PU
lab_meas_PU
Pos_PU
Input Scaling
Speed_PU
2
Speed_fb
Iab_fb_PU
Pos_PU
Iab_meas_PU
Pos_PU
Idq_ref_PU
EnClosedLoop
Duty_Cycles
Control_System1
1
Idq_ref_PU
EnClosedLoop
Vabc_ref
EnPWM
PWM_Duty_Cycles
Output Scaling1
[EnPWM]
Inverter (Code Generation)
Inverter Signals DutyCycles
Inverter (Simulation)
1
Duty Cycles
AURIX TC4x
Pin(s)
Digital Port Write P10
Pins: 6
Loop_Execution
AURIX TC4x
Pin(s)
Digital Port Write P13
Pins: 0
LED_Blink
Ready
View 4 warnings
129%
FixedStepAuto

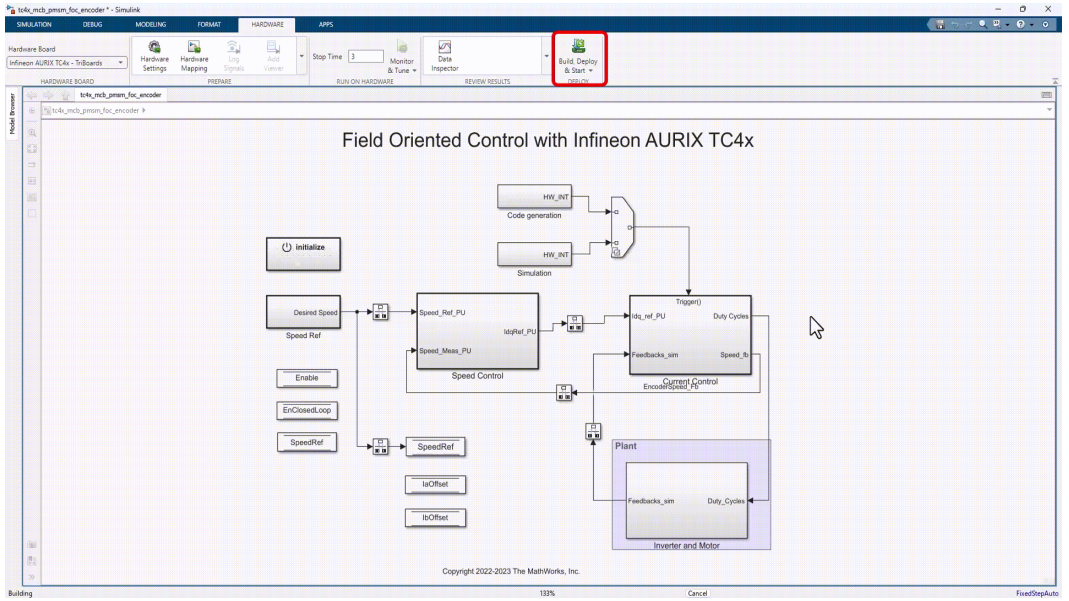

tc4x_mcb_pmsm_foc_encoder/Current Control/ADC/Encoder config * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
SUBSYSTEM BLOCK
Hardware Board
Infineon AURIX TC4x - TriBoards
HARDWARE BOARD
Hardware Settings
Hardware Mapping
Log Signals
Add Viewer
PREPARE
Stop Time
3
Monitor & Tune
RUN ON HARDWARE
Data Inspector
REVIEW RESULTS
Build
DEPLOY
Model Browser
ADC/Encoder config
tc4x_mcb_pmsm_foc_encoder
Current Control
ADC/Encoder config
AURIX TC4x
result
TMADC Pins: AN1, AN2
Iph
Ia_Count
Ia_ADC
Ib_ADC1
EnPWM
IaIb
ADC MidPoint Calibration
1
Iab_EnTicks
2
EnPWM
3
EncSpeed
AURIX TC4x
ticks
speed
Encoder GPT12: 2
Pins: P34_1 P34_2 P34_3
EncoderTicks
uint16
60/(2*pi)/pmsm.N_base
EncoderSpeed
Ready
View 4 warnings
197%
FixedStepAuto


tc4x_mcb_pmsm_foc_encoder/Current Control/Inverter (Code Generation) * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
Hardware Board
Infineon AURIX TC4x - TriBoards
HARDWARE BOARD
Hardware Settings
Hardware Mapping
Log Signals
Add Viewer
PREPARE
Stop Time
3
Monitor & Tune
RUN ON HARDWARE
Data Inspector
REVIEW RESULTS
Build
DEPLOY
Model Browser
Inverter (Code Generation)
tc4x_mcb_pmsm_foc_encoder
Current Control
Inverter (Code Generation)
1
Inverter Signals
PWM Duty Cycles
100
Scale_to_duty in percentages
AURIX TC4x
duty
PWM Gtm ATOM0
Pins: P02_0, P02_2, P02_9
Comp. Pins: P11_6, P02_4, P02_10
50
Trigger
AURIX TC4x
duty
1
PWM Gtm ATOM1
Pins: P14_7
Comp. Pins:--
Ready
View 4 warnings
181%
FixedStepAuto

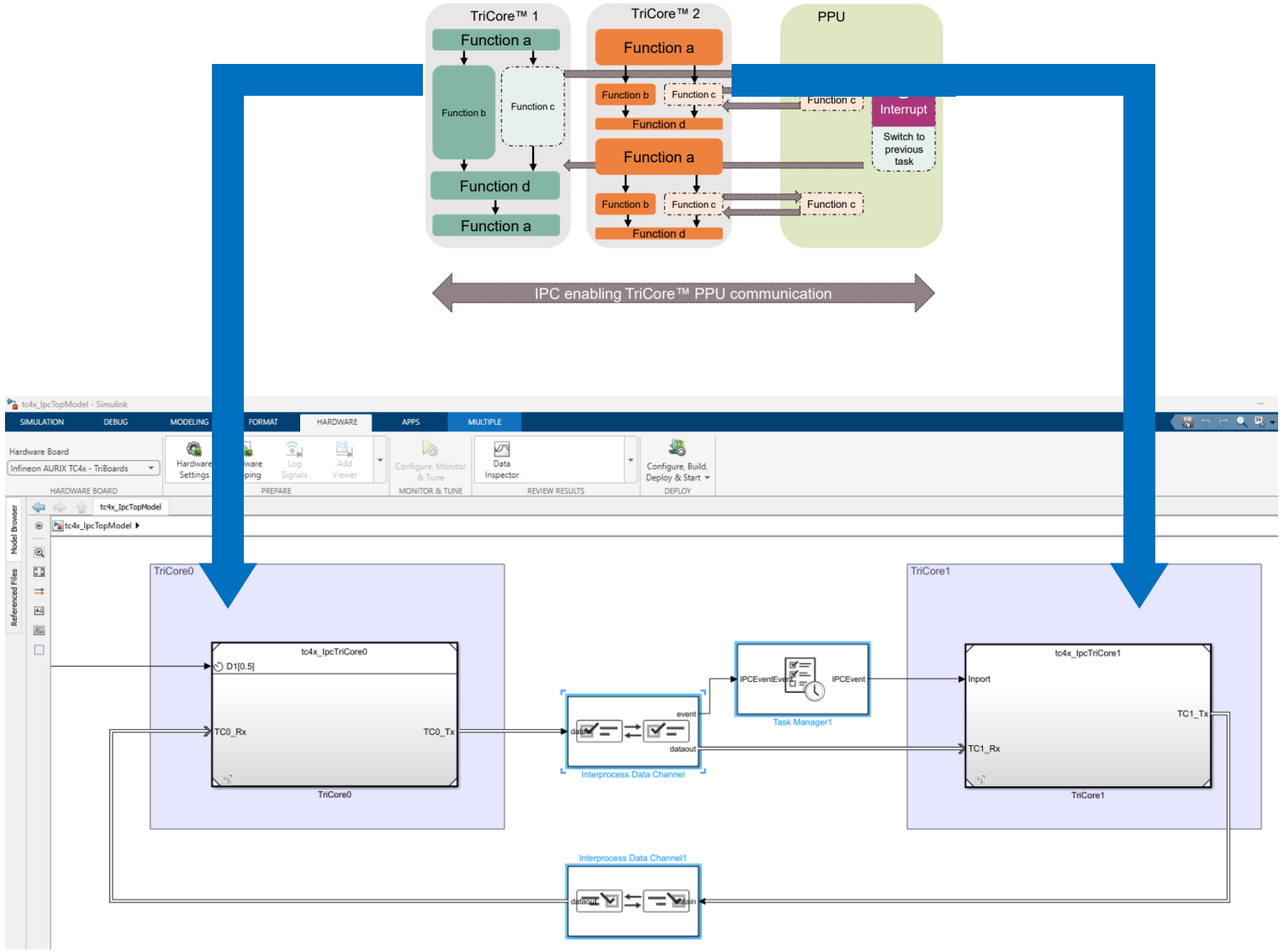
Develop Embedded Software to run on Infineon AURIX™ TC4x hardware using HSP

1. Model → **2. Simulate** → **3. Generate code and run on AURIX**

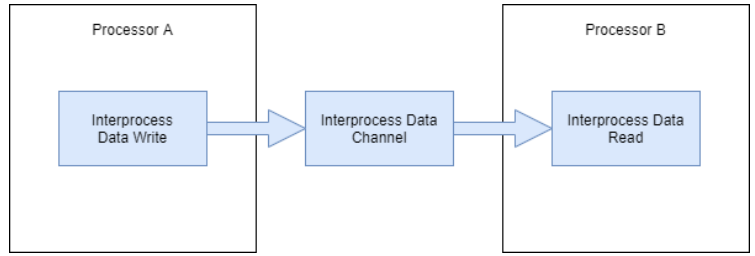




Multi-core modeling using IPC Data Channel Blocks

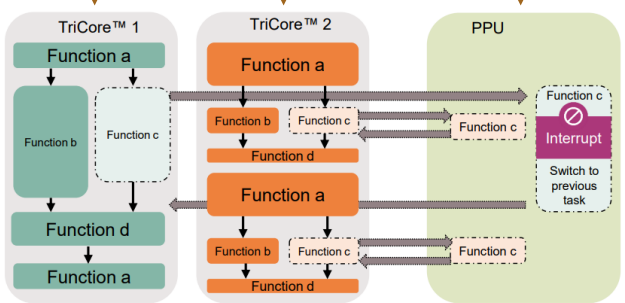


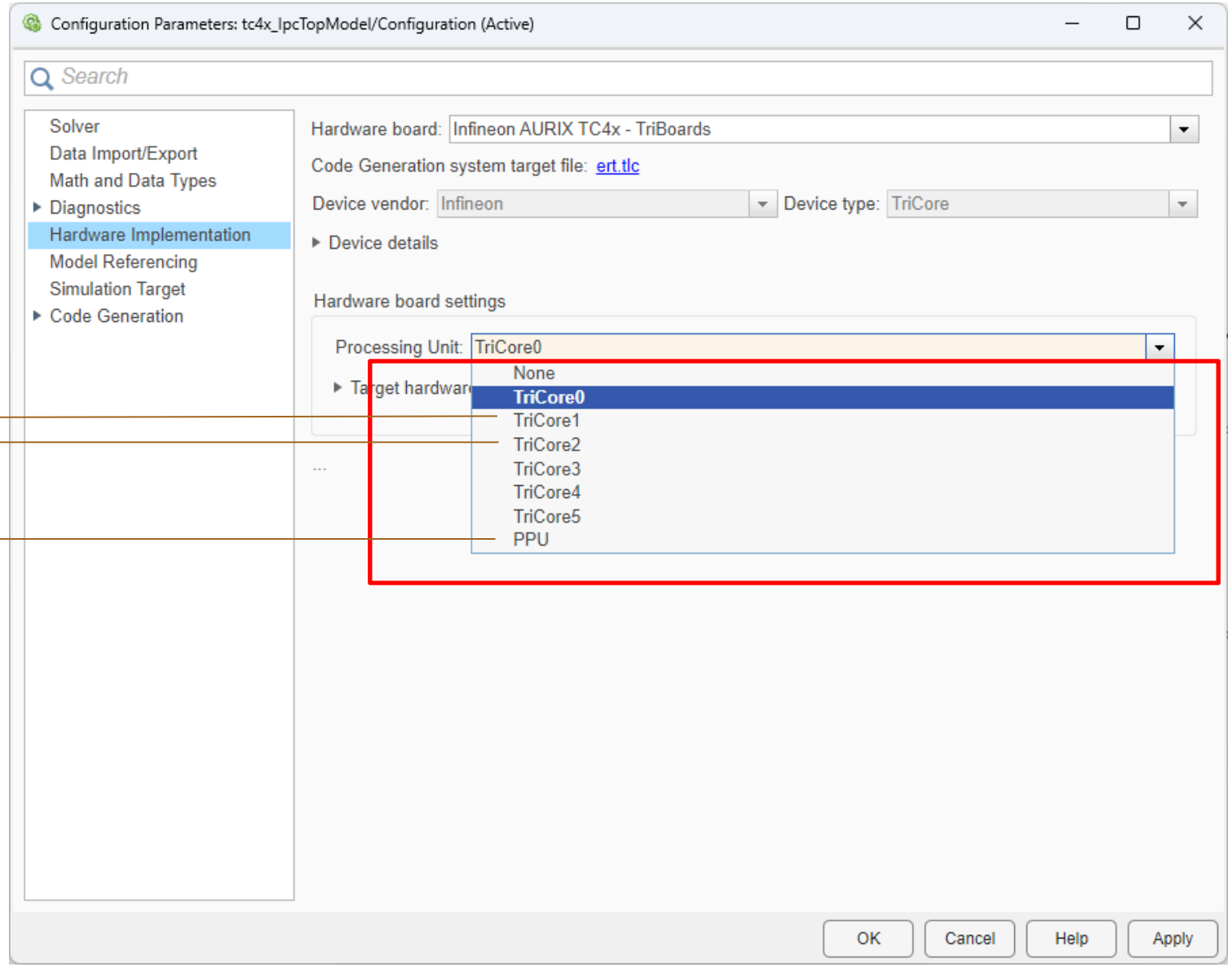
- Interprocess Data Channel Block enables data transfer between multiple cores in AURIX™



- Partition algorithms to run on different cores in single top model reference

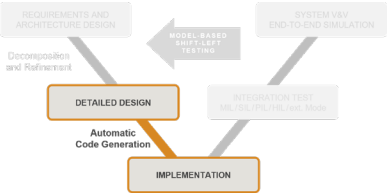
Configure model to generate and run code on specific TriCore™ / PPU

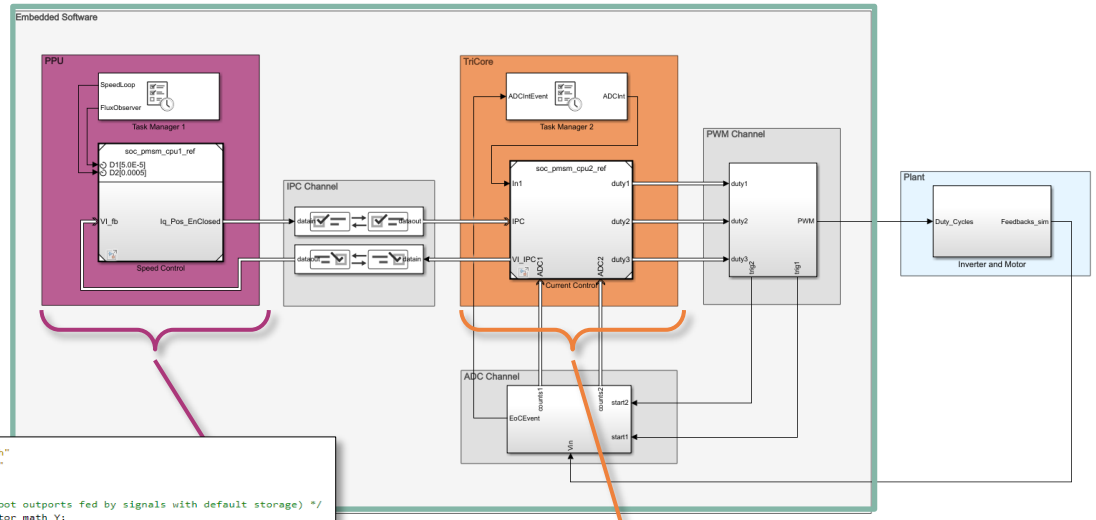




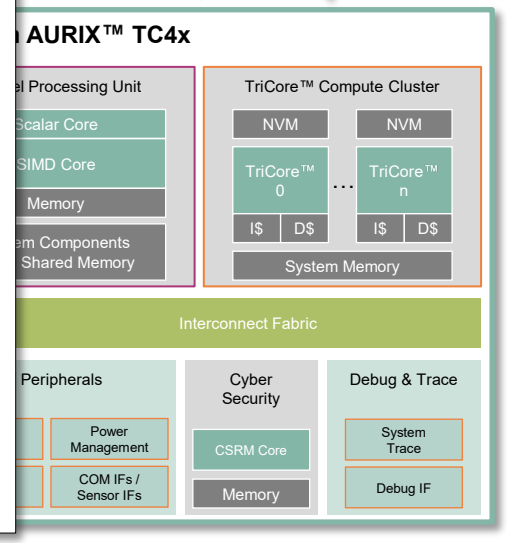
Algorithm implementation by Automatic Code Generation

Infineon AURIX™ TC4x Hardware Support Package






```
#include "vector_math.h"
#include "arc_vector.h"
#include "rtwtypes.h"

/* External outputs (root outports fed by signals with default storage) */
ExtY_vector_math_T vector_math_Y;

/* Real-time model */
static RT_MODEL_vector_math_T vector_math_M_;
RT_MODEL_vector_math_T *const vector_math_M = &vector_math_M_;

/* Model step function */
void vector_math_step(void)
{
  __vccm const real32_T *tmp_0;
  __vccm const real32_T *tmp_1;
  __vccm real32_T *tmp;
  int32_T i;
  for (i = 0; i <= 16; i += 16) {
    tmp = &vector_math_Y.Outa[i];

    /* Sum: '<Root>/Add' incorporates:
     *  Constant: '<Root>/A'
     *  Constant: '<Root>/B'
     *  Outport: '<Root>/Outa'
     */
    tmp_0 = &vector_math_ConstP.A_Value[i];
    tmp_1 = &vector_math_ConstP.B_Value[i];

    /* Outport: '<Root>/Outa' */
    vvst(vvfadd(vvld(tmp_0), vvld(tmp_1)), tmp);

    /* Outport: '<Root>/Outs' incorporates:
     *  Outport: '<Root>/Outa'
     */
    tmp = &vector_math_Y.Outs[i];

    /* Sum: '<Root>/Add' incorporates:
     *  Constant: '<Root>/A'
     *  Constant: '<Root>/B'
     *  Outport: '<Root>/Outa'
     */
    tmp_0 = &vector_math_ConstP.A_Value[i];
    tmp_1 = &vector_math_ConstP.B_Value[i];

    /* Outport: '<Root>/Outs' */
    vvst(vvfsub(vvld(tmp_0), vvld(tmp_1)), tmp);
  }
```



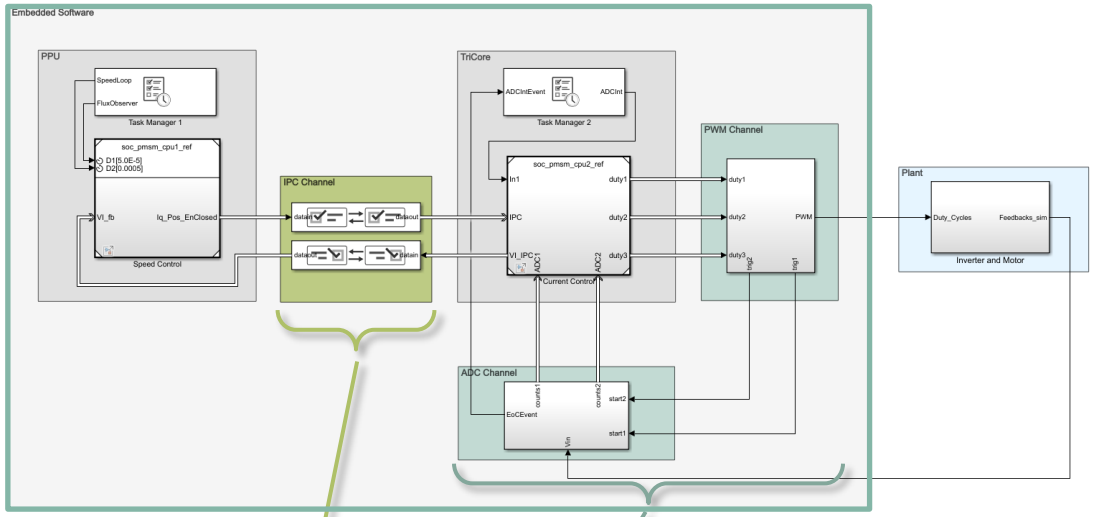
- Enables **target-specific code generation** for the heterogeneous multi-core system
  - Infineon TriCore™
    - ANSI C code generation
  - Parallel Processing Unit (PPU)
    - **Code Replacement Libraries** for math operators using vector implementation based on Synopsys® VDSP library elements
    - **SIMD code generation** using Synopsys® VDSP vector intrinsics and vector math
    - **Automatic VCCM memory allocation** for vector data

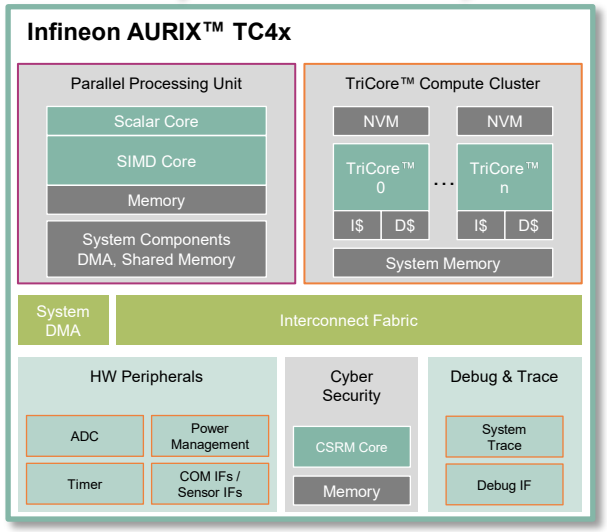
Benefits

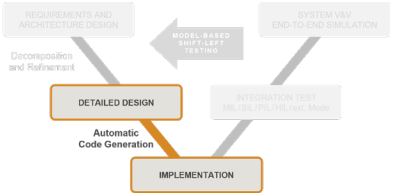
Leveraging PPU for advanced vector algorithms without the need for detailed expertise in parallel programming.

Algorithm implementation by Automatic Code Generation

Infineon AURIX™ TC4x Hardware Support Package





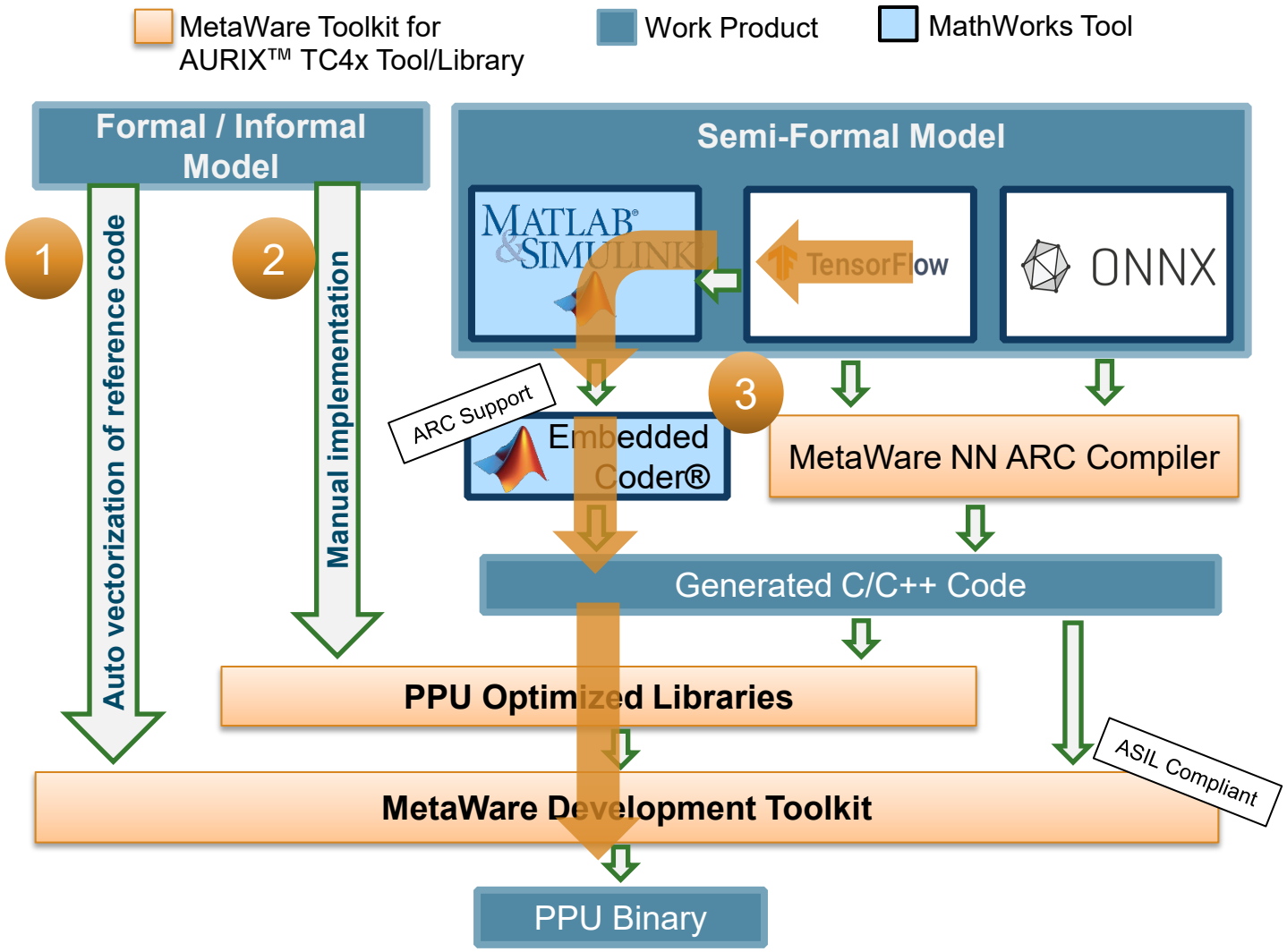


- **Integration** of automatically generated algorithmic code **within the software framework**
  - Library elements for **on-chip peripherals** are replaced by corresponding **parametrized Infineon iLLD function calls** to access these peripherals
  - **Inter-processor communication infrastructure** for data exchange between the processor sub-systems and for triggering the execution on the PPU
  - **Scheduling utilities** to trigger function execution
- **Tool flow automation**
  - Triggering the **compilation of the source code** (.elf) for the different processor sub-systems
  - **Specifying the executable** in the virtual platform
  - **Download of executable** to processor on HW board (flash, RAM)

Benefits

Easy access on on-chip peripherals and automated tool flow including download of executable.

Neural Network Deployment on Infineon AURIX TC4x PPU



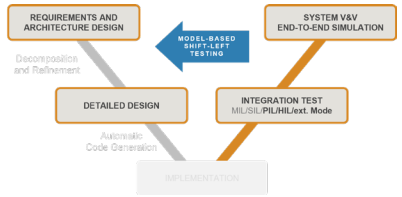
Three approaches to translate NN models to source code:

1. Use language extensions to enable auto-vectorization feature of MetaWare

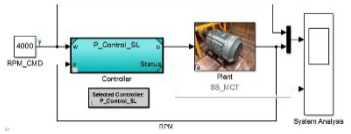
2. Use optimized libraries that provide wide range of functions such as standard C library, DSP and platform-specific runtime

3. Use Model-Based Design support to take full advantage of automatic code generation for TC4x PPU with:
   - TensorFlow or ONNX format passed to MetaWare NN compiler that outputs an optimized C code to compile with MetaWare

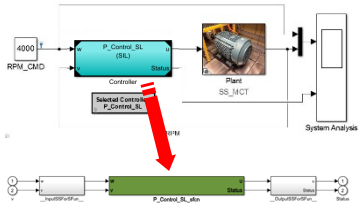
Model-Based Shift-Left Testing enabling early verification



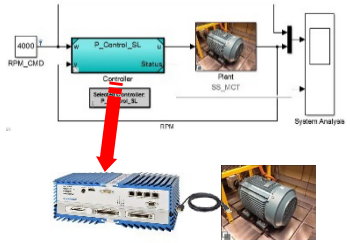
MIL



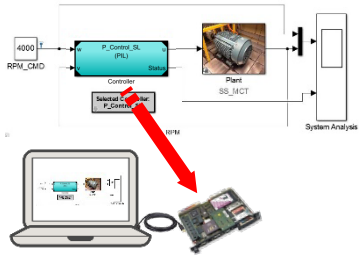
SIL



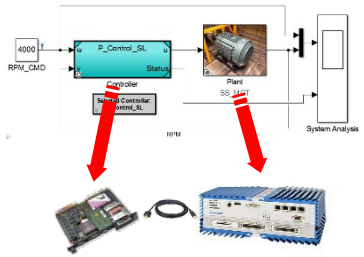
RCP



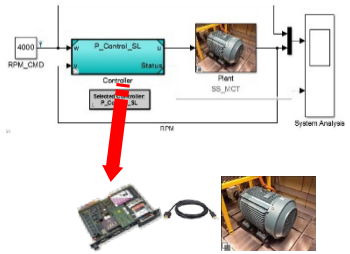
	Non Real-Time	Real-Time
Host (ANSI C)	• Model-in-the-Loop (MIL) • Software-in-the-Loop (SIL)	• Rapid Control Prototyping (RCP)
Target	• Virtual Processor-in-the-Loop (vPIL) • Processor-in-the-Loop (PIL)	• Hardware-in-the-Loop (HIL) • External Mode



(v)PIL



(v)HIL



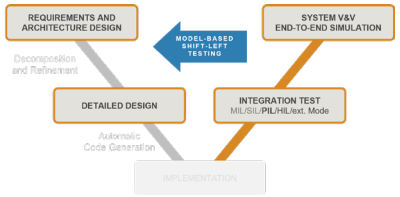
Monitor and Tune

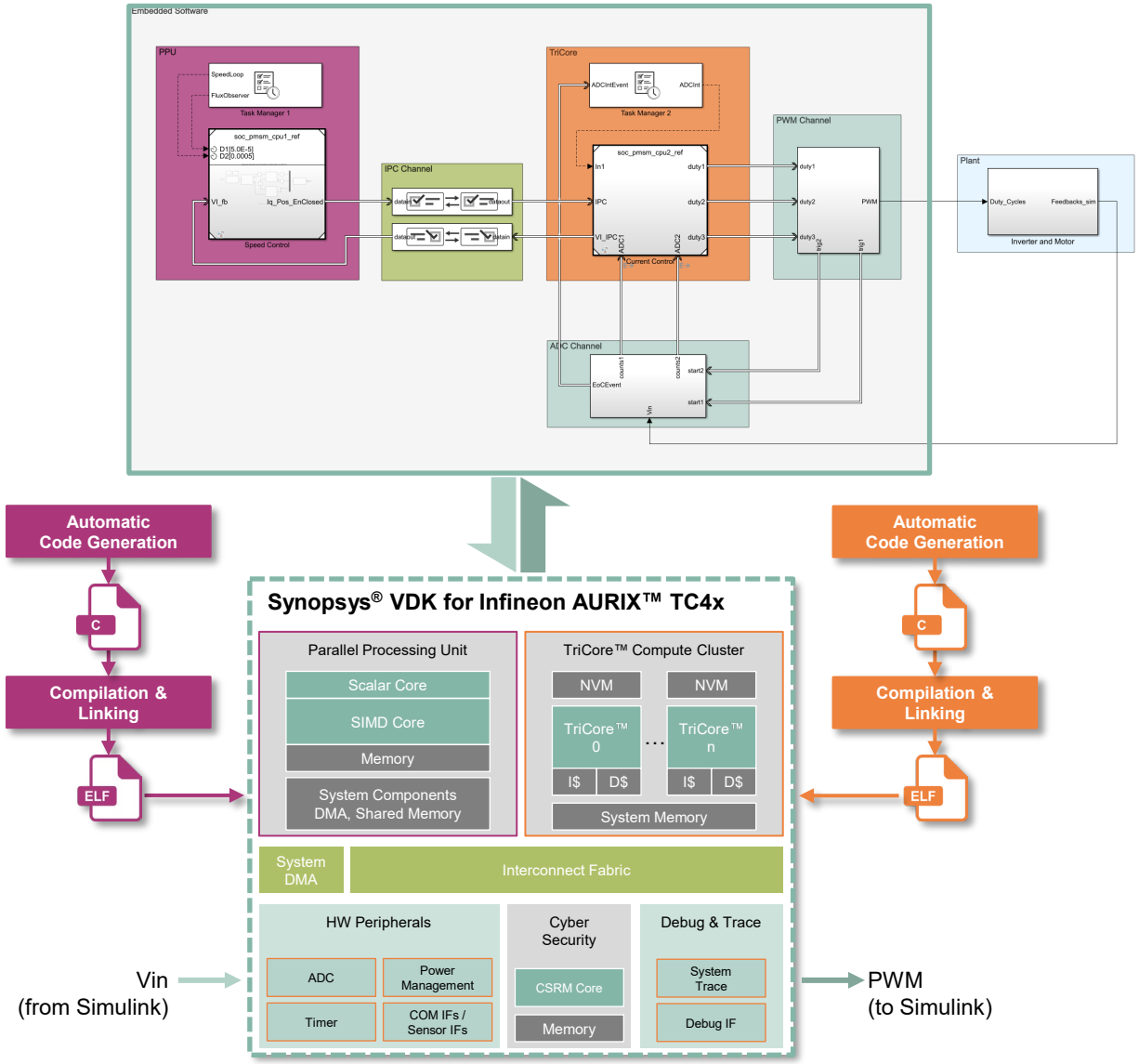
- **Model-in-the-Loop (MIL)**
  Multi-domain simulation of the algorithm within its context (closed-loop, end-to-end).
- **Software-in-the-Loop (SIL)**
  Algorithm running as stand-alone executable (ANSI-C) on host platform called from the multi-domain testbench.
- **Rapid Control Prototyping (RCP)**
  Algorithm running on real-time capable host system connected to the physical hardware.
- **(virtual) Processor-in-the-Loop ((v)PIL)**
  Algorithm running as stand-alone executable (target-specific C code) on a virtual or target platform called from the multi-domain testbench.
- **(virtual) Hardware-in-the-Loop ((v)HIL)**
  Intergrated algorithm (target-specific C code) running in real-time on target platform connected to plant model executed on real-time capable host system.
- **Monitor and Tune**
  Integrated algorithm (target-specific C code) running in real-time on target platform connected to physical hardware. Parameters can be modified from and signal values visualized on host platform.

Benefits

Early defect detection through equivalence / back-to-back teststing between simulation model and implementation as also required by certification standards (e.g. ISO 26262).

Model-Based Shift-Left Testing enabling early verification



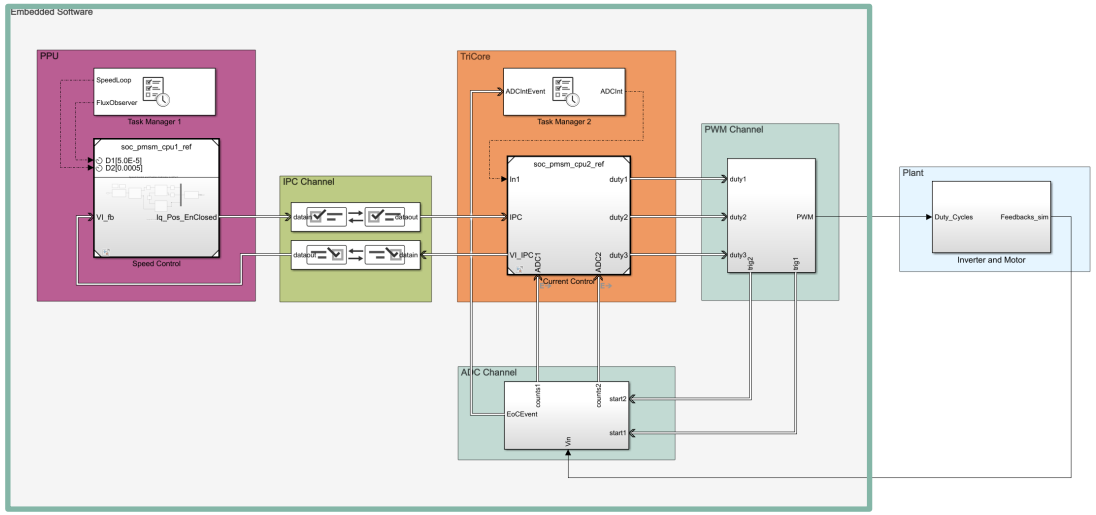


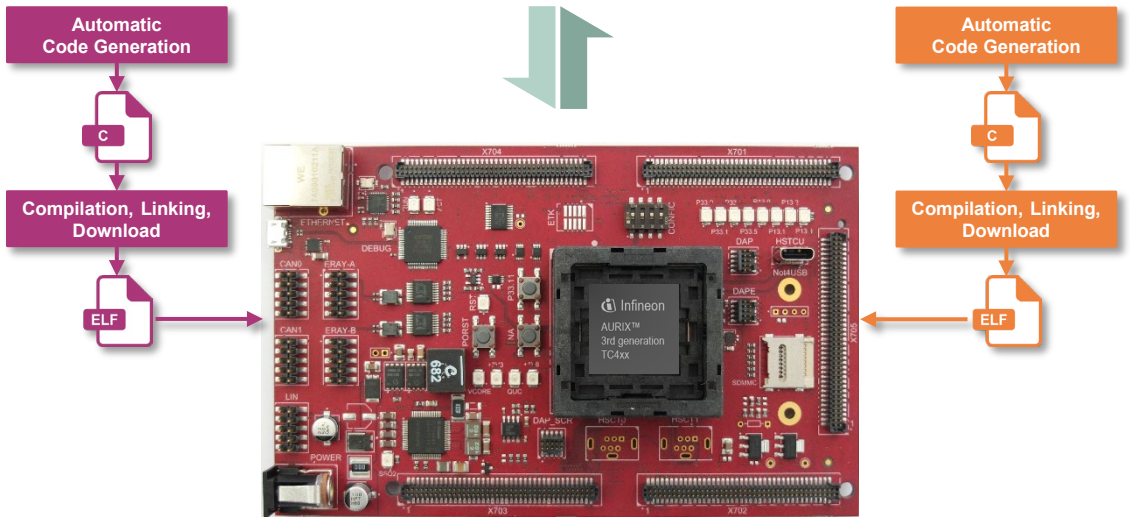
- Co-Simulation with Virtualizer
  - Leveraging the Synopsys® Virtualizer™ Development Kit (VDK) for Infineon AURIX™ TC4x
  - Provides an **executable virtual platform** of the heterogeneous multi-core microcontroller platform, including the TriCore™ and PPU processor sub-systems, on-chip peripheral units, and on-chip system busses
  - **Co-simulation** between the Simulink® testbench and the Synopsys® Virtualizer™ virtual platform **executing the automatically generated, integrated, and compiled code** (i.e. algorithimc code and iLLD calls)
  - Signals can directly be injected or output at the behavioural peripheral models using the Synopsys® VSI interface also verifying the on-chip accessibility

Benefits

Enables early software development and closed-loop verification on register level without requiring the actual physical target device.

Summary





- The **Infineon AURIX™ TC4x and TC3x Hardware Support Packages** enables the efficient use of the heterogeneous multi-core platform through optimized scalar and vectorized code generation (TriCore™, PPU)
- **Model-Based Design** enables the design and early verification of complex applications
- **Automatic C code generation** increases productivity and improves code quality
- **Smooth workflow** through tight integration with other solutions of the Infineon AURIX™ TC4x tool ecosystem

Questions?

Thank You!

Reach out to jprabaka@mathworks.com if you would like to try out

Model-Based Design on Infineon AURIX